INNOVATIONS
IN
VIDEO

FOR.A®

SERVICE MANUAL

NTSC

FA-410

DIGITAL
TIME BASE CORRECTOR

FOR·A COMPANY LIMITED

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DIGITAL
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OPERATION AND TECHNICAL MANUAL

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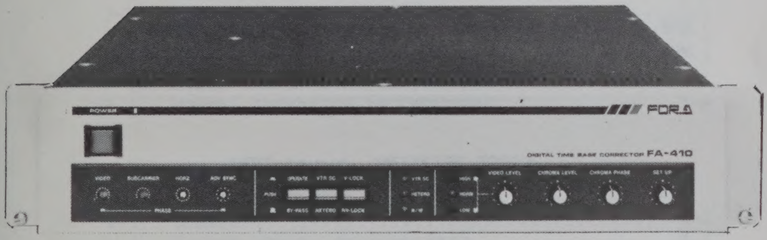
POWER
FOR.A
DIGITAL TIME BASE CORRECTOR FA-410
VIDEO
SUBCARRIER
HORZ
ADV SYNC
PHASE
PUSH
OPERATE
VTR SC
V-LOCK
BY-PASS
HETERO
H/V-LOCK
VTR SC
HETERO
B/W
HIGH
NORM
LOW
VIDEO LEVEL
CHROMA LEVEL
CHROMA PHASE
SET UP

PREFACE

This manual contains information for the operation and service of the FA-410 NTSC *Time Base Corrector manufactured by FOR.A Company Limited.*

The use of this manual is strictly limited for the purpose of installing, operating, maintaining and servicing the FOR.A equipment described within. Any of the information given shall not, in whole or in part, be disclosed to third parties, except as authorized in writing by FOR.A Corporation of America.

FOR.A reserves the right to change the design and specifications contained herein without prior notice.

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GENERAL INFORMATION

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1-1. FUNCTIONAL DESCRIPTION

The FA-410 NTSC is a digital Time Base Corrector developed using the latest technology in combination with extensive experience in developing broadcasting equipment. Time base errors, which generally appear in composite video signals from NTSC heterodyne process VTRs, can be corrected. Dropouts can also be compensated for. The FA-410 can be widely utilized for broadcasting, editing and dubbing applications.

1-2. FEATURES

- High performance and reliability through digital design with 8 bits and 4 times subcarrier.
- Greater Signal-to-Noise Ratio for both luminance and chrominance through signal component digital encoding.
- Full 16 H-line wide time base error correction.
- Wide bandwidth frequency response can be achieved using feedback of VTR subcarrier.
- Vertical Interval Time Code Signals (VITC), Vertical Interval Reference Signals (VIR), etc. can be preserved by selection of V blanking width.
- V-Lock or Non V-Lock mode operation.
- Using the DUB selection switch, dubbing operation from Non V-Lock VTRs to direct VTRs can be performed.
- Standard DOC function.
- Black Burst outputs are available providing wider system flexibility (2 outputs).
- Advanced Sync output; level can be selected to either -4.0 or -0.3 Vpp.

- Built-in RS-170A Sync Generator with Gen-lock function.
- Adjustment of gen-lock timing is easy to do.
- System design enables easy adjustment and system integration.

1-3. CONFIGURATION AND SPECIFICATIONS

The FA-410 is housed in a 3.5" (8.80 cm) high enclosed chassis, which can be installed in a standard 19" equipment rack, or used as a tabletop unit.

The FA-410 consists of the following assemblies (refer to Figure 1-1):

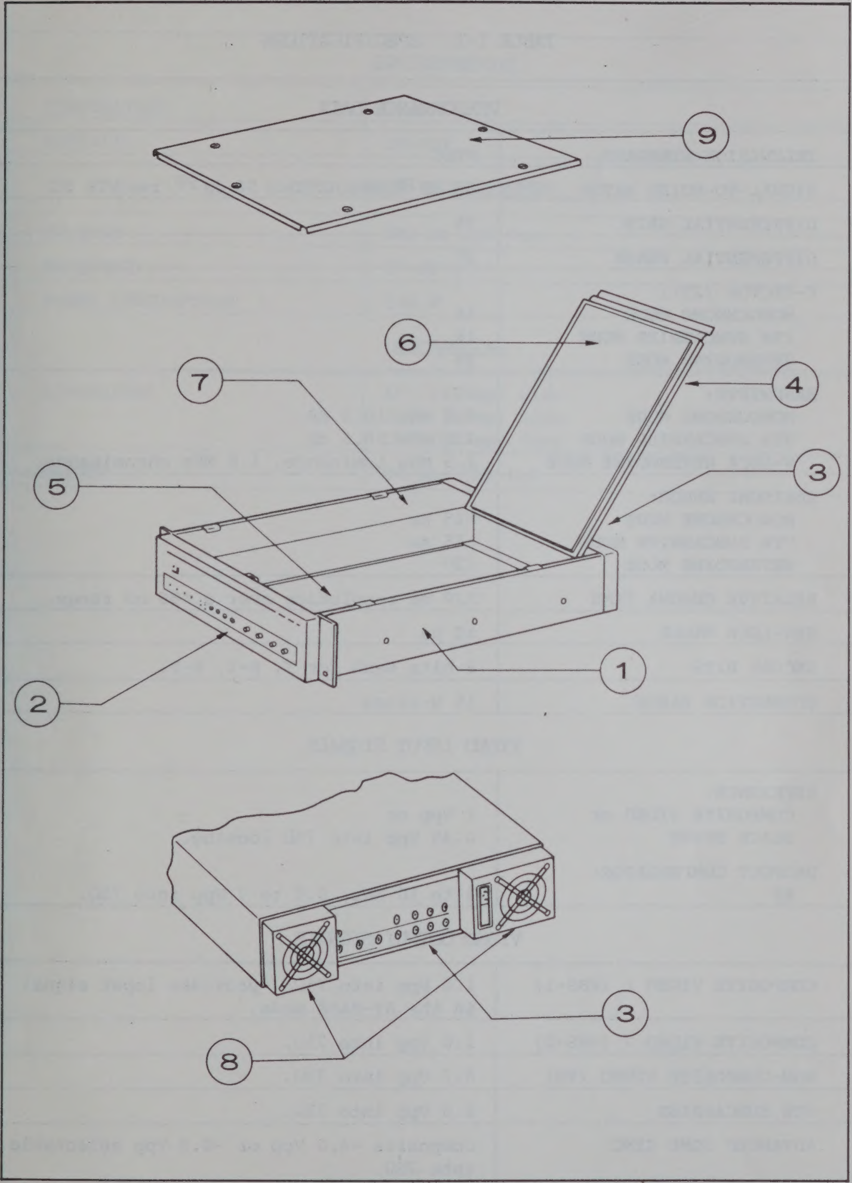
1. FA-410 CHASSIS ASSEMBLY
2. FRONT PANEL ASSEMBLY
    a. FRONT PANEL - most controls and indicators are mounted on this panel.
    b. FRONT PANEL PRINTED CIRCUIT CARD - several system controls are located on this card, accessible by opening the hinged FRONT PANEL.
3. REAR PANEL ASSEMBLY

    Input and Output connectors.
4. INPUT PROCESSOR CARD

    This card is visible by removing the TOP COVER of the unit.
5. MEMORY, MEMORY CONTROL AND DOC CARD

    This card is mounted on the bottom of the unit and is accessible by flipping open the inside plate assembly which is hinged at the rear.
6. OUTPUT PROCESSOR CARD

    This card is attached to the underside of the hinged plate assembly.
7. POWER SUPPLY
8. FANS
9. TOP COVER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4
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1
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3
8

FIGURE 1-1.

TABLE 1-1. SPECIFICATIONS

PERFORMANCE DATA	
TELEVISION STANDARD	NTSC
SIGNAL-TO-NOISE RATIO	58 dB $^{pp}/_{rms}$(HETERO) 56 dB $^{pp}/_{rms}$(VTR SC)
DIFFERENTIAL GAIN	2%
DIFFERENTIAL PHASE	2°
K-FACTOR (2T):	
MONOCHROME MODE	1%
VTR SUBCARRIER MODE	1%
HETERODYNE MODE	3%
BANDWIDTH:	
MONOCHROME MODE	4.2 MHz ±0.5 dB
VTR SUBCARRIER MODE	4.2 MHz ±0.5 dB
V-LOCK HETERODYNE MODE	2.5 MHz Luminance, 1.0 MHz chrominance
RESIDUAL ERROR:	
MONOCHROME MODE	±15 ns
VTR SUBCARRIER MODE	±15 ns
HETERODYNE MODE	±2°
RELATIVE CHROMA TIME	±20 ns resolution over a ±80 ns range.
GEN-LOCK PHASE	±2 µs
ENCODE BITS	8 bits each for Y, R-Y, B-Y.
CORRECTION RANGE	16 H-lines
VIDEO INPUT SIGNALS	
REFERENCE:	
COMPOSITE VIDEO or	1 Vpp or
BLACK BURST	0.45 Vpp into 75Ω looping.
DROPOUT COMPENSATOR:	
RF	3 to 10 MHz, 0.2 to 1 Vpp into 75Ω.
VIDEO OUTPUT SIGNALS	
COMPOSITE VIDEO 1 (VBS-1)	1.0 Vpp into 75Ω; provides input signal in the BY-PASS mode.
COMPOSITE VIDEO 2 (VBS-2)	1.0 Vpp into 75Ω.
NON-COMPOSITE VIDEO (VB)	0.7 Vpp into 75Ω.
VTR SUBCARRIER	2.0 Vpp into 75Ω.
ADVANCED COMP SYNC	Composite -4.0 Vpp or -0.3 Vpp selectable, into 75Ω.
BLACK BURST	Composite 0.45 Vpp into 75Ω (2 outputs).

ENVIRONMENTAL	
TEMPERATURE	0-40° C.
HUMIDITY	10-80%
POWER REQUIREMENTS	
VOLTAGE	100 or 117 Vac
FREQUENCY	50-60 Hz
POWER CONSUMPTION	130 W
MECHANICAL	
DIMENSIONS	17" (430mm) wide 3.5" (88mm) high 19" (505mm) deep
WEIGHT	24 lbs (11 kg)

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INSTALLATION

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2-1. UNPACKING AND INSPECTION

The FA-410 was carefully inspected and fully assembled prior to shipment and is ready for use after installation described in this section.

When unpacking, inspect for damage that may have occurred in shipping. If there is any apparent damage, contact the delivering carrier and FOR.A. Check all parts supplied with the unit according to Table 2-1 below.

TABLE 2-1. FA-410 ACCESSORIES

1 Power Cord
1 spare Fuse (Inset to the behind of front panel.)
1 Rack Slide Kit
1 Operation and Technical Manual

2-2. INSTALLATION

The FA-410 is operated at either 100 V or 117 V, 50/60 Hz ac power. Operation can be selected by a voltage switch card located in the AC receptacle on the rear panel of the unit.

For safety precautions the FA-410 has been outfitted with a 3-prong AC power cable to ground the unit when plugged into a compatible outlet. If a 2-prong outlet is used, a 2-3 prong adapter has to be used, but the green wire should be connected to ground.

The TBC can be used as a tabletop unit or mounted in a standard 19" equipment rack for which a pair of rack mounting slides are included with all units (remove the rubber feet). See Figure 2-1 for installation details.

Avoid operating the unit at locations subject to extremes in temperature, humidity and dust (see Table 1-1. Environmental Requirements). For optimum performance proper air cooling is required. Other equipment should not be placed closer than 2" away from the unit, except when rack mounted. In this case other equipment may be immediately above and below the FA-410 as long as air flow is not blocked at the underside of the front panel and at the rear of the chassis.

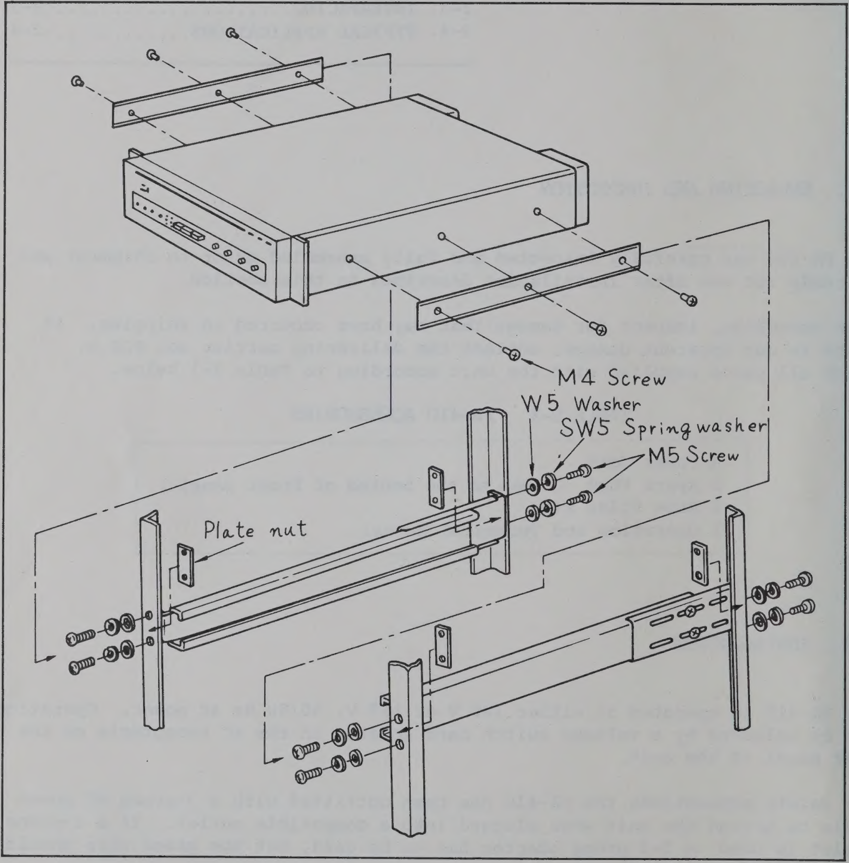

FIGURE 2-1. RACK SLIDES MOUNTING

2-3. INTERFACING

Connect all interface cables to the rear panel connectors of the FA-410 shown in Figure 2-2 and described in Table 2-2. Interconnections should be made with 75 Ω coaxial cable RG-59/U or equivalent, using BNC connectors.

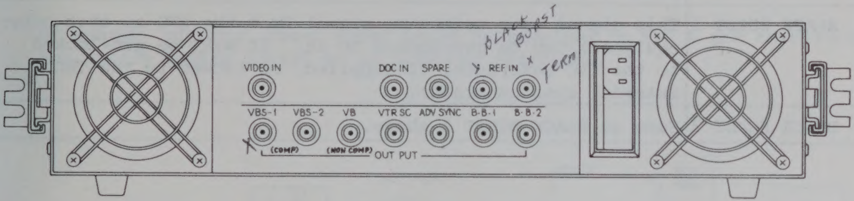

FIGURE 2-2. REAR PANEL, INTERFACE CONNECTORS

TABLE 2-2. REAR PANEL CONNECTORS

CONNECTOR	CHARACTERISTICS AND FUNCTION
VIDEO IN	Accepts 1.0 Vpp video input from a VTR or video disc source. Load impedance is 75 Ω. When the OPERATE/BYPASS switch on the front panel is set to BYPASS or when the AC power is not supplied, the video input signal is connected to VIDEO OUT 1 (VBS-1).
DOC IN	Accepts an RF signal from the VTR. The level required is 0.2 to 1.0 Vpp. Load impedance is 75 Ω.
SPARE	Spare connector.
REF IN	Accepts video or Black Burst Reference signal for gen-lock. Terminate with 75 Ω when not looped through.
VIDEO OUT 1 (VBS-1)	Provides 1.0 Vpp composite video into 75 Ω. This output is switched to the video input in the BYPASS mode (Power off or by selection).
VIDEO OUT 2 (VBS-2)	Provides 1.0 Vpp composite video into 75 Ω. This output is inactive in BYPASS.
NON COMP (VB)	Provides 0.7 Vpp non-composite video (no sync) into 75 Ω.
VTR SC	Provides subcarrier signal with jitter locked to input H sync. By supplying this signal to the VTR, heterodyne color is changed to standard interleaved color in the video output signal. Resolution and K-Factor of the output signal are totally preserved using this mode of operation.

TABLE 2-2. REAR PANEL CONNECTORS (Cont'd).

CONNECTOR	CHARACTERISTICS AND FUNCTION
ADV SYNC	Provides -4.0 Vpp or -0.3 Vpp (selectable inside TBC) comp sync which is in advance of the reference by 8 H lines, nominally. The advance position may be changed by front panel control.
BLACK BURST 1	This signal is a reference signal from the TBC so that other equipment can be gen-locked to it. It will be gen-locked to the TBC reference, if supplied, or locked to the TBC internal sync generator.
BLACK BURST 2	Same as BLACK BURST 1 above.

2-4. FA-410 TYPICAL INSTALLATIONS AND APPLICATIONS

1. INTERFACING WITH A SWITCHER

Figure 2-3 shows a typical application using an FA-410 in conjunction with a switcher and other video equipment.

The Playback VTR is shown connected to the TBC with DOC, VTR SC and ADV SYNC interfaces. This is a general case and in some circumstances either DOC, or VTR SC, or both may not be used. (Paragraph 4 and 5 of this section describe these individual cases in more detail).

ADV SYNC must be used to generate a synchronous corrected video signal to mix with other video sources as is shown.

Also shown is a camera, which could be used for adding titles or program origination. It has been gen-locked to the switcher using Black Burst.

A Video Character Generator, in this case the FOR.A VTW-600, has also been shown in this system. It can be used in either an up-stream keying mode to add titles to any source going into the switcher, or to add them to the FA-410 Video Output prior to switching.

2. A-B ROLL EDITING

Figure 2-4 shows a typical A-B roll editing installation using two FA-410 TBCs.

TBC A's internal sync is the reference for this system. TBC B is gen-locked to A via the Black Burst output from TBC A, and this Black Burst is supplied to a camera source, which might be used for titles or program, and to a video character generator in this case a FOR.A VTW-300.

The switcher is gen-locked via Black Burst from TBC A. The switcher and all inputs, therefore, have been made synchronous with TBC A's sync so that switching is clean with no rolls or other such disturbances.

VTR C records the output from the switcher.

Of course, external Black Burst could be supplied to TBC A and therefore the entire system locked to an external reference.

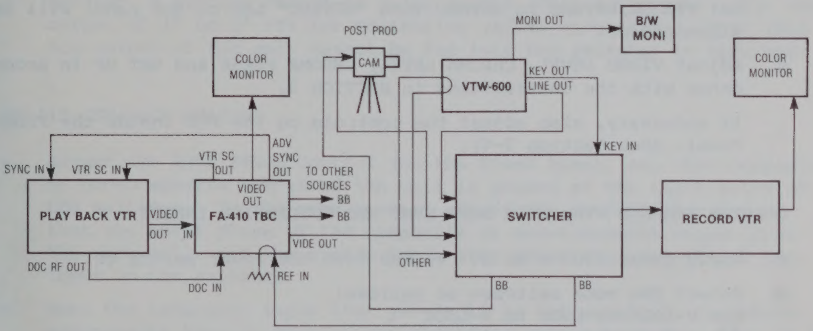
POST PROD
MONI OUT
B/W MONI
COLOR MONITOR
CAM
VTW-600
KEY OUT
LINE OUT
COLOR MONITOR
ADV SYNC OUT
VTR SC OUT
SYNC IN
VTR SC IN
KEY IN
VIDEO OUT
TO OTHER SOURCES
BB
BB
PLAY BACK VTR
VIDEO OUT
IN
FA-410 TBC
SWITCHER
RECORD VTR
VIDE OUT
OTHER
DOC RF OUT
REF IN
DOC IN
BB
BB

FIGURE 2-3. INTERFACE WITH SWITCHER

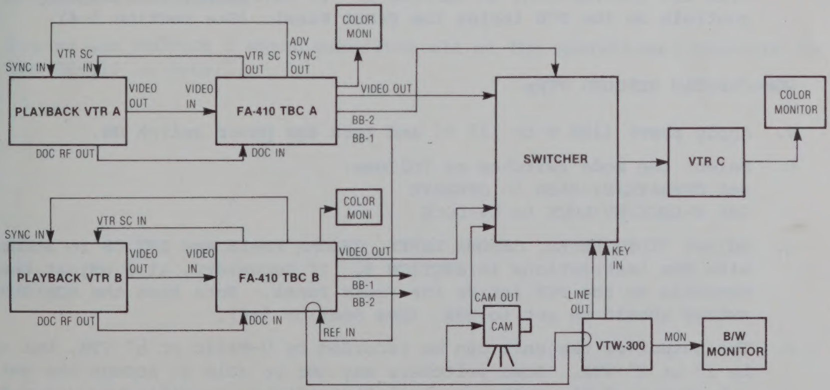
COLOR MONI
ADV SYNC OUT
VTR SC IN
VTR SC OUT
SYNC IN
PLAYBACK VTR A
VIDEO OUT
VIDEO IN
FA-410 TBC A
VIDEO OUT
BB-2
BB-1
DOC RF OUT
DOC IN
SWITCHER
COLOR MONITOR
VTR C
COLOR MONI
VTR SC IN
SYNC IN
PLAYBACK VTR B
VIDEO OUT
VIDEO IN
FA-410 TBC B
VIDEO OUT
BB-1
BB-2
KEY IN
CAM OUT
LINE OUT
CAM
DOC RF OUT
DOC IN
REF IN
VTW-300
MON
B/W MONITOR

FIGURE 2-4. A-B ROLL EDITING

3. EDITING AND DUBBING APPLICATIONS

At times it is necessary that 3/4" and 1/2" VTRs which cannot accept an external reference be dubbed either to 3/4" or 1" VTRs. The FA-410 can perform these functions in the NV-LOCK mode. Refer to paragraphs 6 and 7 which describe these steps in detail.

4. CAPSTAN SERVOED VTRs WITH SYNC INPUT BUT NO SUBCARRIER INPUT

a. Apply power (100 V or 117 V) and turn the power switch ON.

b. Select the mode switches as follows:
Set V-LOCK/NV-LOCK to V-LOCK
Set OPERATE/BY-PASS to OPERATE
Set VTR SC/HETERO to HETERO (the "HETERO" LED on the panel will be illuminated).

c. Adjust VIDEO LEVEL, CHROMA LEVEL, CHROMA PHASE and SET UP in accordance with the instructions in SECTION 3.

If necessary, also adjust the controls on the PCB inside the Front Panel. (See Section 3-4).

5. CAPSTAN SERVOED VTRs WITH BOTH SYNC AND SUBCARRIER INPUTS

a. Apply power (100 V or 177 V) and turn the Power switch ON.

b. Select the mode switches as follows:
Set V-LOCK/NV-LOCK to V-LOCK
Set OPERATE/BY-PASS to OPERATE
Set VTR SC/HETERO to VTR SC (the "VTR SC" LED will be illuminated).

c. Adjust VIDEO LEVEL, CHROMA LEVEL, CHROMA PHASE and SET UP in accordance with the instructions in SECTION 3. If necessary, also adjust the controls on the PCB inside the Front Panel. (See Section 3-4).

6. NON-CAPSTAN SERVOED VTRs

a. Apply power (100 V or 117 V) and turn the power switch ON.

b. Select the mode switches as follows:
Set OPERATE/BY-PASS to OPERATE
Set V-LOCK/NV-LOCK to NV-LOCK

c. Adjust VIDEO LEVEL, CHROMA LEVEL, CHROMA PHASE and SET UP in accordance with the instructions in SECTION 3. If necessary, also adjust the controls on the PCB inside the Front Panel. Note that the NOR-DUB switch should be set to NOR. (See Section 3-4).

d. The output of the unit can be recorded by U-Matic or ½" VTR, but not by 1" or 2" VTR. Some switchers may not be able to accept the output signal of the unit, so check the switcher specifications carefully prior to incorporation.

7. NON CAPSTAN SERVOED VTRs
(WHEN DUBBING TO THE DIRECT COLOR TYPE VTRs 1" or 2")

a. Apply power (100 V or 117V) and turn the power switch ON.

b. Select the mode switches as follows:
Set OPERATE/BY-PASS to OPERATE
Set V-LOCK/NV-LOCK to NV-LOCK
Set NOR/DUB to DUB (control inside the Front Panel - see SECTION 3).

c. Adjust VIDEO LEVEL, CHROMA LEVEL, CHROMA PHASE and SET UP in accordance with the instructions in SECTION 3. If necessary, adjust the controls on the PCB inside the Front Panel. (See SECTION 3-4).

d. The output of the unit can be dubbed to the direct color type VTRs (1"or 2"). If the output of the unit is directly fed into the color monitor, a picture cannot be color-locked (this is normal). Use the output of 1" or 2" VTR for monitoring (after recording). Note that the output of the unit cannot be fed into the switcher in this mode.

8. FA-410 GEN-LOCK PHASING

a. Adjust the HORZ PHASE Control (on the Front Panel) so, that composite or non-composite output of the unit is phased at the input point of the switcher. In the same manner, adjust the SC PHASE Control so that the burst phase of the composite or non-composite output from the unit will meet the system subcarrier phase requirements at the input to the switcher.

b. When the reference input (for gen-lock) is not supplied, the above adjustments have no meaning and therefore cannot be made. Also in the NV-LOCK mode, these adjustments cannot be made.

9. OTHER FA-410 CONTROLS

Please see SECTION 3 which describes all of the operational controls for the FA-410 in detail.

SECTION 3

OPERATION

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3-6. NORMAL OPERATION PROCEDURES......3-6

3-1. GENERAL

The operating controls of the FA-410 NTSC are divided into two areas; front panel accessible controls (described in paragraph 3-2 and 3-3 and shown in Figure 3-1), and less frequently used controls and adjustments found on the inside (described in paragraph 3-4 and 3-5 and shown in Figure 3-2).

After the description of these available controls and adjustments this section concludes with the Operation Procedures of the FA-410 TBC (paragraph 3-6).

3-2. MODE SELECTION AND INDICATORS - FRONT PANEL

OPERATE/BY-PASS:

In the BY-PASS mode, the video input signal supplied to the unit is by-passed and generated from the VIDEO OUTPUT 1 (VBS-1) connector. In the OPERATE mode, composite video output is generated from the VIDEO OUTPUT 1 and 2 (VBS-1, -2), while non-composite video output is generated from NON COMP (VB) video output connector.

VTR SC/HETERO:

The HETERO mode is used with capstan servoed VTRs which do not accept external subcarrier. The LED indicator is illuminated while this mode is selected. The VTR SC mode is used with capstan servoed VTRs which accept external subcarrier. The LED indicator is illuminated while this mode is selected.

V-LOCK/NV-LOCK:

The NV-LOCK mode is used with non-capstan servoed VTRs. The V-LOCK mode is used with capstan servoed VTRs.

VIDEO LEVEL INDICATORS

High/Normal/Low levels are indicated by LEDs.

3-3. CONTROLS - FRONT PANEL

VIDEO LEVEL

If either High or Low LEDs are illuminated, pull out the control and adjust it properly until Normal LED is illuminated. By pushing the control in, unity gain is selected.

CHROMA LEVEL:

By pulling the control out, level adjustments can be made. Pushing the control in, unity chroma gain is selected.

CHROMA PHASE:

The variable range of this control is 180°. For additional range, use the 180° switch (HETERO or VTR SC - refer to SECTION 3-4 which describe these controls) on the Front Panel PCB. By pulling the control out, it becomes a variable adjustment, by pushing it in, normally correct phase is selected.

SET-UP:

By pulling the control out, it becomes a set-up control. Pushed in, it is preset to normal NTSC set-up.

VIDEO PHASE:

Adjusts the picture position of the output signal relative to the output sync.

SC PHASE:

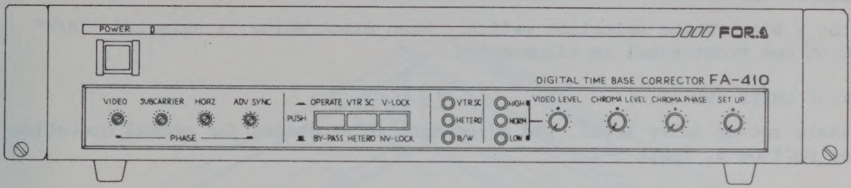
Adjusts the subcarrier phase of the output chroma and burst relative to subcarrier phase of the external reference signal. The range is greater than 180°. By combining with the 180° switch on the Front Panel PCB, over 360° of range can be obtained.

HORZ PHASE:

Adjusts the phase of the output sync ± 2 μsec relative to the horizontal sync of the external reference signal.

ADV SYNC PHASE:

Adjusts the phase of Advanced Sync supplied to the VTR over a range of -2H to -14H relative to external reference in 2H steps. Generally, it should be set to -8H.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VTR SC
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NORM
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VIDEO LEVEL
CHROMA LEVEL
CHROMA PHASE
SET UP

FIGURE 3-1. FRONT PANEL

3-4. CONTROLS - INSIDE FRONT PANEL (ON PCB)

Following controls and adjustments are accessible by opening the front panel door. (See Figure 3-2).

VTR SC 180° (SW 1):

Switches VTR subcarrier phase (supplied to VTR) to 180°.

HETERO 180° (SW 2):

Switches subcarrier phase to 180°, so that the hue range is extended to 360°. It is normally NOT necessary to change the position of this switch.

SC 180° (SW 3):

Switches subcarrier phase of the built-in sync generator by 180° so that the range is extended to 360°. This is used in conjuntion with the front panel SUBCARRIER PHASE control.

GEN LOCK SC (SW 4):

Generally it should be set to NORMAL. When subcarrier phase of the reference input is not standard and gen-lock operation is not stable, it should be switched to the other position.

NOR/DUB (SW 5):

When the time base corrected signal from a NV-LOCK VTR is recorded on direct record type VTRs, set the switch to DUB. When the corrected signal is recorded on other type VTRs such as U-Matics, set the switch to NORMAL.

DOC ON/OFF (SW 6):

Dropout Compensator operation ON/OFF switch.

COLOR/BW (SW 7):

Color - Black/White selection switch. When Black/White is selected, "B/W" LED on the Front Panel is illuminated.

SET-UP UNITY (VR 1):

Adjusts set-up unity level. No adjustment is necessary for normal operation (see SECTION 5, Table 5-2).

SET-UP SUB (VR 2):

Adjusts the variable set-up range. No adjustment normally necessary. See SECTION 5, Table 5-2).

VTR SC (VR 4):

Adjustment is necessary to "phase" the TBC and VTR on initial installation. No other adjustment in necessary, unless VTR or cable between TBC and VTR are changed. For procedure, see SECTION 3-5).

CHROMA PHASE (ϕ) UNITY (VR 5):

Adjusts chroma phase unity. No adjustment necessary for normal operation. See SECTION 5, Table 5-2).

CHROMA PHASE SHIFT RANGE (VR 6 and VR 8):

These adjust the variable range of chroma phase shift. No operating adjustment is normally necessary. See SECTION 5, Table 5-2).

CHROMA LEVEL UNITY (VR 9):

Adjusts chroma level unity gain. No operating adjustment is normally necessary. See SECTION 5, Table 5-2).

CHROMA LEVEL SUB (VR 10):

Adjusts the variable range of chroma level. No operating adjustment is normally necessary. See SECTION 5, Table 5-2).

VIDEO LEVEL UNITY (VR 12):

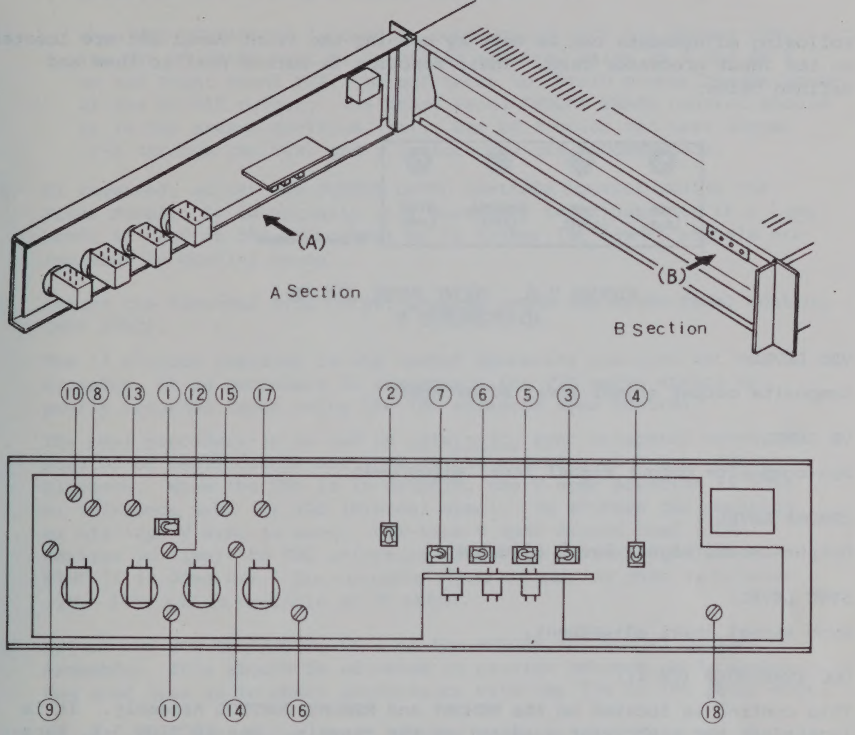
Adjusts the video level unity gain. No operating adjustment is normally necessary. See SECTION 5, TABLE 5-2).

VIDEO LEVEL SUB (VR 13):

Adjusts the variable range of video level. No operating adjustment is normally necessary. See SECTION 5, Table 5-2).

VIDEO PHASE SUB (VR 15):

Adjusts the variable range of video phase. No operating adjustment is normally necessary. See SECTION 5, Table 5-2).



A Section detail

① VTR SC 180° (SW 1)
② HETERO 180° (SW 2)
③ SC 180° (SW 3)
④ GEN LOCK SC (SW 4)
⑤ NOR/DUB (SW 5)
⑥ DOC ON/OFF (SW 6)
⑦ COLOR/BW (SW 7)
⑧ SET-UP UNITY (VR 1)
⑨ SET-UP SUB (VR 2)
⑩ VTR SC (VR 4)
⑪ CHROMA PHASE UNITY (VR 5)
⑫ CHROMA PHASE SHIFT RANGE (VR 6)
⑬ CHROMA PHASE SHIFT RANGE (VR 6)
⑭ CHROMA LEVEL UNITY (VR 9)
⑮ CHROMA LEVEL SUB (VR 10)
⑯ VIDEO LEVEL UNITY (VR 12) VR 8
⑰ VIDEO LEVEL SUB (VR 13)
⑱ VIDEO PHASE SUB (VR 15)

FIGURE 3-2. FRONT PANEL INSIDE CONTROLS AND ADJUSTMENTS A

3-5. OTHER INSIDE CONTROLS AND ADJUSTMENTS

Following adjustments can be made by opening the Front Panel and are located on the Input processor Card. Their function is marked next to them and defined below:

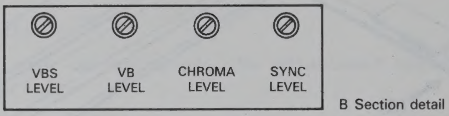


FIGURE 3-3. FRONT PANEL INSIDE ADJUSTMENTS B

VBS LEVEL:

Composite output signal level adjustment.

VB LEVEL:

Non-composite output signal level adjustment.

CHROMA LEVEL:

Output chroma signal level adjustment.

SYNC LEVEL:

Sync signal level adjustment.

DOC THRESHOLD (VR 1):

This control is located on the MEMORY and MEMORY CONTROL Assembly. It is located in the right rear quadrant of the chassis. See SECTION 3-6, Paragraph 6).

3-6. NORMAL OPERATION PROCEDURES

SECTION 2 has described the basic installation and set up procedure which select the proper operating modes associated with various applications and system configurations in which the FA-410 can be used. Therefore it is assumed that these are already set correctly.

The following steps should be taken to finalize system integration.

1. Adjust SC PHASE using the Front Panel control in conjunction with SC 180° (SW 3) on the Front Panel inside PCB assembly. This will phase the burst of the FA-410 with other sources into a switcher.

2. Adjust H PHASE using the Front Panel control, to horizontally phase the FA-410 output into a switcher.

3. When VTR SUBCARRIER is used in conjunction with the source VTR, the VTR SC PHASE must be initially adjusted using VR 4 and SW 1 on the Front Panel PCB. Adjust these to obtain proper chroma phase at the FA-410 output. The Front Panel CHROMA PHASE control should be in the preset position (in). Use of a color bar test signal (E-E through the VTR) and a vectorscope are recommended).

4. If required, adjust the OUTPUT LEVEL controls located inside the Front Panel. It is normally only necessary to adjust them if a long cable is used at the TBC output or if higher (or lower) signals are required in special cases.

5. Adjust the Advanced Sync Output phasing using the Front Panel control (ADV SYNC).

   The 11 o'clock position is the normal operating position but on occasion, it is necessary to compensate for VTR servo errors or poorly recorded tapes using the TBC advanced sync control.

   The best procedure is to use an externally sync triggered waveform monitor or oscilloscope and look at the position of V sync during playback. When the TBC is in OPERATE, the V sync position is that of reference sync (or TBC internal sync). In BY-PASS the position of off-tape V sync is seen. Off-tape V sync should lead (occur earlier in time) the TBC reference sync by 8 H lines. Adjust ADV SYNC if it does not. The variable range of the ADV SYNC is between -2H~-14H, and is variable in 2H steps.

6. Adjust the DOC THRESHOLD, VR 1 on the MEMORY and MEMORY CONTROL Assembly. This should be adjusted to provide optimum performance. One good test is to check performance with the VTR in the pause mode.

7. Adjust VIDEO and CHROMA LEVEL, CHROMA PHASE and SET UP using the Front Panel procamp controls as necessary.

   The preset (in) position always represents "unity" gain or 1:1 output with respect to the input signal.

WITH THESE THREE SECTIONS OF THE FA-410 MANUAL ALL INFORMATION HAS BEEN GIVEN TO INSTALL AND OPERATE THE FOR.A FA-410 NTSC DIGITAL TIME BASE CORRECTOR AND TO ACHIEVE THE BEST PERFORMANCE OF THE SYSTEM.

THE FOLLOWING TWO SECTIONS ARE DEVOTED TO THE TECHNICAL ASPECTS OF THE TBC WITH DETAILED EXPLANATION OF THE ASSEMBLIES, MAINTENANCE AND ALL NECESSARY SCHEMATICS.

SECTION 4

THEORY OF OPERATION

4-1. GENERAL..........................4-1
4-2. SYSTEM THEORY OF OPERATION.......4-1
4-3. FUNCTIONAL DESCRIPTION:
INPUT PROCESSOR..................4-4
MEMORY, MEMORY CONTROL AND DOC...4-7
OUTPUT PROCESSOR.................4-8

4-1. GENERAL

The theory of operation of the FA-410 NTSC described in this section is divided into two parts. The first describes the overall operation in a broad sense and is called SYSTEM THEORY OF OPERATION. This part is followed by another section which describes the operation of each function in more detail and is called the FUNCTIONAL DESCRIPTION.

4-2. SYSTEM THEORY OF OPERATION

The following technical description is divided into five basic parts, which apply to the five different functions of the system, each on its separate subassembly. (Refer to the SYSTEM BLOCK DIAGRAM A2-3591 in SECTION 6):

INPUT PROCESSOR
MEMORY, MEMORY CONTROL AND DOC
OUTPUT PROCESSOR
FRONT PANEL (OPERATION) AND REAR PANEL (INTERFACE)
POWER SUPPLY AND CHASSIS

INPUT PROCESSOR

This part of the system processes the input video signal to prepare it for analog-to-digital conversion. Also several important timing pulses are generated in this assembly.

The video input signal is passed through a buffer amplifier and after going through overall video level and chroma level control circuits, is divided into three paths. One path goes to the color process circuit for the HETERO color mode. Another goes to the low pass filter (4.5 MHz) which passes the luminance signal in the HETERO color mode and the composite video signal in the VTR SC mode. The last one goes to the level detector.

The video signal, after going through the low pass filter (4.5 MHz) is further divided into two paths: one to the direct-coupled amplifier which is used in the VTR SC mode; the other to the direct-coupled amplifier and low pass filter (2.7MHz) circuit which is used in the HETERO color mode. A feedback clamp signal is connected to these two amplifiers to provide DC restoration.

The output of the above two circuits is supplied to an A/D converter after selection of the respective mode. The output of one A/D converter is supplied to the DOC and MEMORY.

The following operations are performed in the color process circuitry for the HETERO color mode:

- The input video signal is separated into luminance and chroma components,
- the separated chroma signal is demodulated into the color difference signals, R-Y and B-Y,
- the R-Y and B-Y color difference signals are time division multiplexed,
- after clamping this signal to a reference level it is supplied to an A/D converter, and
- the output of the A/D converter is supplied to the DOC and MEMORY.

Several circuits are used in the following operations to generate required timing pulses:

- H and V sync separation from the input video signal,
- generation of clamp pulse, burst gate pulse, and H sample pulse,
- generation of frame pulse from V sync,
- generation of 4 x f_{SC} reference frequency from the H-locked VCO circuit,
- generation of 4 x f_{SC} write clock and VTR SC which is supplied to VTR,
- generation of other timing pulses needed by the MEMORY CONTROL.

MEMORY, MEMORY CONTROL AND DOC

The MEMORY employs 4K static RAMS to store the digitized video signal. Sufficient capacity is provided to store 16H lines of data. Composite video is stored in the VTR SC mode, and component video is stored in the HETERO color mode. The maximum memory data rate is approximately 2 MHz. The read/write cycle is approximately 1 µs.

The MEMORY CONTROL is the heart of the system. All read/write cycle timing is based on clock, phased H, V sync (Field divided by 2) and other such control signals from both the read and write sides of the system.

The DROPOUT COMPENSATOR (DOC) is composed of three sections:

- Detection of dropouts from the VTR playback RF signal envelope,
- storing the digital video signal, and
- controlling the data replacement.

In the HETERO color mode, data which is 1H earlier is used to fill in for dropouts. In the VTR SC mode, data which is 2H earlier is used.

OUTPUT PROCESSOR

The OUTPUT PROCESSOR contains the primary functions of: D/A conversion, output signal processing, and reference sync generation.

In the HETERO color mode, the D/A converted luminance signal and R-Y and B-Y component signals after modulation onto the reference subcarrier are filtered and added together to form the composite color video signal.

In the VTR SC mode, the composite digital signal is D/A converted directly.

Other operations include: the addition of sync and burst, adding blanking and providing level control functions.

The system sync generator is another part of the OUTPUT PROCESSOR. The sync generator will gen-lock to external sync, or internally generate all required sync and subcarrier signals.

FRONT PANEL (OPERATION) AND REAR PANEL (INTERFACE)

On the FRONT PANEL are located all of the normally routine controls, switches and indicators. (See SECTION 3).

On the REAR PANEL are all of the necessary input/output connectors. The bypass/operate relay switch is also included. (See SECTION 2-3).

POWER SUPPLY AND CHASSIS

A switching regulator is utilized for the d.c. power supply. A noise reduction function is included in this unit.

The chassis is designed to be compact in size and light weight yet sufficiently strong. Other mechanical features include ease of maintenance and troubleshooting when required.

4-3. FUNCTIONAL DESCRIPTION

INPUT PROCESSOR
(REF. BLOCK DIAGRAM A2-3540)

The INPUT PROCESSOR Assembly consists of five major functions:

Y/C SEPARATION,
A/D CONVERSION,
SYNC DETECTION,
INPUT VCOs, and
FINAL OUTPUT AMPLIFIER

Y/C SEPARATION
(REF. SCHEMATIC A2-3488)

The video input signal is buffered at Q1 and passes through the overall video gain control (PC1). The gain-controlled video signal is connected to the group delay correction circuitry, consisting of Q2 and Q3 and then goes to the chroma level control circuit which is primarily IC1.

The video signal is then routed to three paths:

First to the color process circuit which is composed of Q30 - Q40. This circuit is used in the HETERO color mode. The video signal is buffered at Q30 and is connected to the bandpass filter which is composed of L10, L11, C32, C33 and C34, so that chrominance signal is separated. This signal is decoded to the color difference signals, B-Y and R-Y, by IC5. Each is passed through a low pass filter and clamp circuit. These signals are later supplied to the A/D converter.

The R-Y signal is connected to the burst gate circuit (Q40), then to the burst-locked VCO consisting of a crystal oscillator and error amplifier (IC6), so that the VCO subcarrier signal is phased-locked to the burst of input video signal. From the VCO subcarrier signal, two subcarriers with a 90° phase difference, B-Y subcarrier and R-Y subcarrier, are produced and connected to the IC5 decoder.

The second path is to the low pass filter (4.5 MHz). The video signal is buffered at Q8 and band-limited by the low pass filter, composed of L3, L4, C9, C10 and C11.

Then it is amplified by Q9 and Q10, and further routed to 3 circuits as noted:

- One is to the direct-coupled amplifier (Q12 - Q14) which is operative in the VTR SC and MONOCHROME modes,
- one is to the luminance signal circuit which is operative in the HETERO color mode. In this mode, the video signal luminance-to-chroma delay time is corrected by DL-1 and then amplified by Q27 and Q28. Then it is connected to a 2-step group delay correction circuit which is composed of Q17 - Q20. The video signal is then amplified (Q23 - Q 25) and passed through the low pass filter (2.7 MHz) which is composed of L7 - L9 and C20 - C26. In each of the direct coupled circuits, the video signal is DC-clamped to a fixed voltage, and supplied to the

A/D converter. IC2 is used to select the path, based on the mode of operation.

- One path is to the Start Up Sync Separation circuit. More details about this circuit will be described in the SYNC DETECTION section.

The third path is to the level detection circuit. More details will be described in the SYNC DETECTION section.

A/D CONVERTION
(REF. SCHEMATIC A2-3489)

VIDEO SIGNAL CIRCUIT

The video signal which is selected by IC2 (Y/C PROCESSOR), composite color video signal in the VTR SC mode, or luminance signal in the HETERO color mode and B/W mode, is connected to IC9 (A/D converter), through an amplifier which is composed of Q45 - Q47. The video signal is converted to digital form and is latched by IC11 and supplied to the memory through J7.

CHROMINANCE SIGNAL CIRCUIT

The two color difference signals, R-Y and B-Y, which are supplied from the Y/C PROCESSOR, are time division multiplied using 2 sets of 4 diode bridges. The switching clock for the multiplexing operation is shaped from a 2 x f_{SC} clock by IC13 and Q51 - Q55. The multiplexed color difference signal is amplified and level-controlled by Q56, Q57 and Q58, and is clamped to a fixed voltage by a circuit which consists of Q59 - Q61. Then it is supplied to an analog switch (IC14). In the HETERO mode this switch connects the multiplexed color difference signal to the A/D converter (IC10) through an amplifier which is comprised of Q48 - Q50.

In the VTR SC mode, a DC reference voltage (set by VR16) is selected by IC14 and connected to IC10 by the same amplifier path. IC10 converts multiplexed color difference signal to digital in the HETERO color mode, while it is operative as a part of the black clip circuit in the VTR SC mode. Details of the black clip circuit follow.

BLACK CLIP CIRCUIT

The signal input level to both A/D converters used in the system is in a range from 0 to -2V. In the HETERO color mode, the undesired signals in luminance below blanking are automatically clipped when the pedestal of the luminance signal is set to 0V. Peak white is at -1.8V. Therefore, the black clip operation is performed. In the VTR SC mode, signals below blanking are passed through the A/D converter. Sync tip is set to 0V and peak white is at -1.8V. Signals below pedestal are generally chrominance signals and noise produced from the VTR. The black clip circuit detects noise, but lets the chrominance signal pass. Signals below the pedestal except chrominance signals, are passed through the chroma trap circuit (L15 and C62) and supplied to a voltage comparator (IC8) to be compared with a reference voltage.

When signals larger than the reference voltage are supplied to IC8, positive and negative TTL pulses are generated. These TTL pulses operate IC12 and select the digitized DC voltage set by VR16 which has been supplied to IC10 (A/D converter). So if a signal below blanking other than chroma is present, it is clipped and the previously set DC voltage replaces it.

SYNC DETECTION
(REF. SCHEMATIC A2-3490)

FEEDBACK CLAMP

The feedback clamp operates by comparing the voltage which was sampled on the back porch of the video input signal with a set reference voltage, and feeding back an error voltage to the direct-coupled amplifiers in the Y/C PROCESSOR. This reference voltage is adjusted by the SET UP UNITY potentiometer (VR1) on the Front Panel Assembly (2811-1) so that blanking of the video input signal at TP10 (input of IC9, A/D CONVERTER) is 0V in the HETERO color mode. In the VTR SC mode, it is set by the SET UP SUB 1 potentiometer (VR21), so that sync tip of video input signal is at 0V at TP10. Also in the VTR SC mode, if no input signal is supplied, the reference voltage is adjusted by the SET UP SUB 2 potentiometer (VR22) so that the voltage at TP10 is -1V.

SYNC SEPARATION CIRCUIT 1 (START SYNC SEPARATION)

The video input signal from the Y/C PROCESSOR is low pass filtered (L17, C83, C84) and amplified by Q67. The amplified signal is sync-tip clamped (D17) and then supplied to a voltage comparator (IC 17). A TTL level sync signal appears at output of IC17 (TP15).

SYNC SEPARATION CIRCUIT 2 (MAIN SYNC STRIPPER)

The video input signal which has been DC restored by the feedback clamp operation, is supplied to a voltage comparator (IC20). The reference voltage for this comparator is generated by the following circuit.

A voltage which is the sampled back porch level of the video input signal is buffered by IC21 and appears at TP18. The sync tip level of the video input is sampled and hold at Q74 and C100, is buffered by IC21 and appears at TP17.The sync slicing level is the voltage between TP17 and TP18 (Voltage divided by VR24) and is the reference voltage to IC20. The separated sync signal output of the voltage comparator (IC20), is used to generate the H sampling pulse (IC3B, 4D, 4C and 6C), the color clamp pulse (IC1D and Q18) and V sync pulse (Q72 and IC20). The frame pulse (IC5C, 4C and 5D) is generated from V and H sync pulses, and the Field divided by 2 pulse is generated from IC5E.

LEVEL DETECTION CIRCUIT a) up to serial No. 940250

The videoinput signal from the Y/C PROCESSOR is amplified by Q65. Then it is clamped by D11, and this voltage is compared with two different reference voltages using two voltage comparators (IC16). The outputs of these voltage comparators, IC2E, IC3D and 3C control the HIGH, NORM and LOW LEDS on the Front Panel which illuminate corresponding to the video input signal level.

LEVEL DETECTION CIRCUIT b) from serial No. 940251

The input video signal from the Y/C PROCESSOR is amplified by Q65 and supplied to D11, where it's Sync Tip is peakclamped and supplied to two voltage comparators of 1C16. The two reference voltages generated by R236, R238 and R237 are fed, respectively, to the previous two voltage comparators.

The outputs of the two voltage comparators of 1C16 are supplied to the corresponding retrigger multivibrators. The two retrigger multivibrators detect the output level appearing on the two voltage comparators.
By distinguishing the outputs from the multivibrators with 1C1E, 3C and 3D, the LED lamps of HIGH, NORM and LOW are illuminated corresponding to the video input signal level.

INPUT VCO
(REF. SCHEMATIC A2-3491)

4 f_{SC} OSCILLATOR CIRCUIT (14.3 MHz)

The Frequency of this LC oscillator is controlled by L20, VC2 and D16 and the output signal is distributed through IC22. One output is connected to the divide by 910 counter, composed of 4J, 4H and 4F, so that an H rate pulse can be obtained. Another 14.3 MHz signal is supplied to the MEMORY CONTROL from IC22 as the Write Clock. Yet another 14.3 MHz signal is used to clock the phased H, 65H divided by 2 and $\overline{\text{65H divided by 2}}$ signals, Y clock. $\overline{\text{Y clock}}$ and chroma mux clock pulses are generated in conjunction with output of the divide by 910 counter.

The VTR SC signal used for certain VTRs in the VTR SC mode is generated by dividing the 14.3 MHz clock by 4 and controlling the phase of the 4 field sequence. The signal is then passed through a phase shift circuit using IC1A and IC1B. These adjust the VTR SC phase.

The counter output of 5F is phase-shifted by IC6D and supplied to the ramp generator comprised of Q83, Q84, Q87 and Q88. This signal is the ramp reset used in generating the H ramp. The ramp is sampled by a pulse which is generated from video input signal (Q89, Q90, Q85 and C141). The sampled error voltage is amplified by IC24 and connected to a varactor diode (D16), so that the 4 f_{SC} VCO is locked to the H sync of video input signal.

VIDEO PHASE ADJUSTMENT CIRCUIT

The Video Phase is adjusted by varying the amplitude of the above ramp signal. The voltage from the video phase potentiometer is buffered by IC23 and supplied to Q84 of the ramp generator. Adjustment is made using VR30 (VIDEO PHASE SUB 1) in the HETERO color mode, VR32 (VIDEO PHASE SUB 2) in the VTR SC mode, and VR33 (VIDEO PHASE SUB 3) in the NV-LOCK mode.

FINAL OUTPUT AMPLIFIER
(REF. SCHEMATIC A2-3492)

This amplifier consists of a low pass filter, phase equalizers, white clipper, sync mixing circuit, burst mixing circuit and 2 output amplifier stages for the output video signals. The first output stage is for composite video (VBS-1 and VBS-2) while the second output stage is for non-composite video (VB). VIDEO LEVEL, SYNC LEVEL, and BURST LEVEL are all adjustable.

MEMORY, MEMORY CONTROL AND DOC
(NO BLOCK DIAGRAM IS REQUIRED)

MEMORY
(REF. SCHEMATIC A2-3409 and A2-3410)

Digital information converted from the input video, is stored using 4K static RAMS. The 14.3 MHz, 8 bit data supplied from the INPUT PROCESSOR is connected to a serial/parallel converter and converted to parallel data at a rate of approximately 1 MHz. The converted parallel data is supplied to 28 memory ICs. Write and read operations for these ICs are controlled by the MEMORY CONTROL. On the read cycle, data is read from the memory ICs and converted back to serial data at a 14.3 MHz rate.

MEMORY CONTROL
(REF. SCHEMATIC A2-3408)

All of the timing pulses which are needed by the memory operation of the FA-410 are generated in this section. They are: write/read designation pulse, address designation pulse, timing signals for serial-to-parallel conversion and timing signals for parallel-to-serial conversion. Shift registers are used to generate concise timing.

DROPOUT COMPENSATOR
(REF. SCHEMATIC A2-3407)

Four static RAMS are used to continually store data which is used if a dropout is generated in playback signal. Data from 1H or 2H earlier is substituted for missing data.

The 8 bit digital data is latched by IC7T and IC6T. Four memory ICs which are 8N, 8P, 8R and 8S, store digital data. Dropouts, generated in VTR playback signal, are detected by the dropout detector and a dropout pulse is generated. This signal inhibits the data from being written into memory during a dropout and earlier data already stored in the memory ICs is used. In the HETERO color mode, 1H earlier digital data is used. In the VTR SC mode, 2H earlier data is used. Switching is done by IC8L and IC10N.

DROPOUT DETECTOR

Dropout detection is accomplished by detecting a low rf envelope signal from the VTR. This signal is buffered by Q1 and amplified by Q2. Then it is rectified by D1 and D2 and supplied to a voltage comparator (IC2). IC1 is a reference voltage buffer. When the VTR signal is too low, a dropout pulse is generated from the IC2 voltage comparator.

OUTPUT PROCESSOR
(REF. BLOCK DIAGRAM A2-3449)

The OUTPUT PROCESSOR reads out digital data from memory by using clock pulses which are locked to the reference sync signal, and generates analog video signal outputs. The system composition is as follows:

GEN-LOCK CIRCUIT, which synchronizes video output at the FA-410 with a reference signal including the sync separation and sync pulse generation circuits,

SYNC GENERATION, for internal sync and gen-lock to input video for the NV-LOCK mode operation,

MEMORY SYNCHRONIZATION SIGNALS, which operate the memory in synchronization with the reference signal, D/A CONVERSION, which converts digital signals, read out from the memory, to analog signals,

VIDEO PROCESSING, which processes these signals to standard video output signals.

GEN-LOCK CIRCUITRY
(REF. SCHEMATIC A2-3443)

The Sync Separation circuit, which separates sync from the reference signal and the Subcarrier Phase Control circuit, are included in this assembly.

The reference signal is supplied to Q1 buffer amplifier and amplified by Q9 - Q11 after passing through a low pass filter. Then it is DC restored by using a sync tip clamp. The composite sync signal is obtained from IC2-pin1. The V sync signal is separated by an integration circuit and a comparator (IC2-pin 8).

From the stripped sync signal, burst flag, the clamp pulse, H sync and a sync presence detection signal are generated by pulse generators IC6H, 6F, 2J, 3K, 4N, 4F, 5M, 3J and 4J. If a reference signal is detected, the built-in sync generator is gen-locked to it. Q3 and Q5 amplify only the subcarrier frequency. In addition, only the burst signal is gated by Q4 and supplied to a phase comparator (IC11). There, it is compared in phase with the internally generated subcarrier and an error voltage generated which locks a VCO. (See Schematic A2-3445).

SYNC GENERATION
(REF. SCHEMATIC A2-3445 and 3444)

IC8 is the Master Sync Generator. There are three sync modes: V-lock internal sync, V-lock gen-lock and NV-lock mode. Each mode is switched by control circuits.

INTERNAL SYNC
The output at a crystal oscillator (14.3 MHz) is supplied to IC8. IC8 generates subcarrier, sync, horizontal drive, vertical drive, and other timing signals, by taking this 14.3 MHz signal as a reference.

GEN-LOCK
The system is gen-locked to a reference input signal. The crystal VCO is synchronized with an external burst signal. The hysteresis circuit (see Schematic A2-3444) which is composed of Q13 - Q15, IC3, 6P and 5P, corrects the phase relationship between subcarrier, generated by the VCO and external sync by switching a delay circuit to prevent color phase jitter.

H sync is clocked with 2 f_{SC} in a latch circuit (IC3N) and resets the counter (IC2P and 2R) for 2 f_H clock generation.

The counter generates horizontal sync information by counting down 2 f_{SC}.

The phase at 2 f_H is compared with subcarrier phase in IC3N and a color frame signal is generated.

In IC5N (see Schematic A2-3445) odd/even field signal is generated from V and H sync pulses and Field divided by 4 is obtained with reference to the color frame pulse.

With reference to A2-344, the 2 f_H pulse also loads counters IC1N and 1M. These ICs control H phase. Using the H PHASE control on the Front Panel, these counters are preset and H sync delayed in steps on 280 ns. The H signal, which is phase-shifted by IC1N and 1M is supplied to IC8S which provides a phase adjustment in 70 ns steps. Then the H signal is phase-shifted by the H PHASE FINE control which consists of IC5 and IC10S. Then it is connected to the V reset of IC8.

Refering to Schematic A2-3445, the 2 f_H clock signal is counted by IC2M, 2L and 2K and supplied to IC8 as V sync signal.

The Advanced Sync Output is generated by a signal which is more advanced than the Reset signal and resets a counter (IC1L). This counter is clocked every 2H. By presetting the counter using a Front Panel control, the phase of the Advanced Sync Output can be adjusted in 2H steps. The signal generated by IC1L is connected to the advanced sync circuit comprised of IC5L and IC10.

The Advanced Sync signal is amplified by Q30 - Q32. JP5 is generally set to 0 - 1 and the output is -4.0 Vpp. The output is -0.3 Vpp if it is set to 0 - 2.

The blanking signal generator is composed of IC3D, 4D, 5A and 5B. the phase and width of H blanking are adjusted by IC3D. Blanking can be set to ON or OFF every 1H during V blanking from the 10th to 20th H line using IC5A and 5B. This permits VITC or VITS signals to be passed in the vertical interval.

NV-LOCK

IC10, sync signal generator, provides Advanced Sync in the V-LOCK mode. In the NV-LOCK mode, it is used as sync generator which is locked to the V sync signal of the off-tape video input to the FA-410.

In the V-LOCK mode, H sync and V sync are locked by reference video sync pulses.

The V sync output of IC10 is connected to IC6J and Q24, amplified by Q25 and generates a saw-tooth wave determined by the constant-current circuit of IC5, Q26 and C97.

The V sync signal, from input video, gates a part of this saw-tooth signal using Q27, Q28 and Q29. It is then amplified by IC12 and the output voltage controls the VCO frequency and locks it to input video. IC10 is phased so that an 8H delay occurs between the output timing and the tape V sync. The H and V sync pulse outputs at IC8 are gen-locked to IC10. The phase relationship between subcarrier and H sync are compared by the phase detector in IC8. The difference voltage from this detector controls the 14.3 MHz oscillator, composed of L11 and C59. This subcarrier is therefore synchronized with tape V and varies with VTR playback speed. This locks the read clock.

The time base corrected signal chrominance, however, is modulated using subcarrier which has been generated by an independent 3.58 MHz oscillator associated with IC10. In this case, NOR/DUB switch (SW5) on the Front Panel PCB should be set to NOR. SW5 should be set to DUB when dubbing to a direct color VTRs such as a 1" Type C format. In this case, subcarrier is controlled by the VCO associated with IC8.

MEMORY SYNCHRONIZATION SIGNALS
(REF. SCHEMATIC A2-3444)

Several synchronization signals, required by the MEMORY CONTROL, are generated. The H sync pulse is selected by IC4L corresponding to the operation mode. Using this signal, IC25 is reset and synchronized and divides 4 f_{SC} by 7. Then this signal is divided by 2 at IC3R and goes to the memory control as the 65 H pulse. This signal becomes the read address clock and is used to retrieve data from memory. The H sync pulse which is phased with subcarrier by clocking it with 4 f_{SC} at IC3H, is supplied to the MEMORY CONTROL as Phased H. Then its positive edge is used (generated by IC4F and 2F) as a reset pulse for the divide by 2 (IC3R) counter to generate the 65H pulses and also to reset the clock generators for the D/A converter. These signals are the R-Y, B-Y and Y clocks.

D/A CONVERSION
(REF. SCHEMATIC A2-3444 and A2-3446)

The 8 bit digital video signal which is read out from the memory has different formats in the VTR SC mode and HETERO color mode.

In the VTR SC mode, the composite video signal is directly A/D converted and written in and read from memory in this format. However, in the HETERO color mode, component encoding is used. The luminance signal and R-Y and B-Y color difference signals are time multiplexed and provided to and read from the memory. Therefore it is necessary to D/A convert each of these three signals separately.

With reference to Schematic A2-3446-6, the clock generation circuit which consists of IC2E, 2F, 1E and 1F generates these clock signals with timing synchronized to the Phase H signal.

With reference to Schematic A2-3446-6, in the VTR SC mode, 4 f_{SC} is the read clock. D/A converter, IC13, is used to convert the composite video signal in the VTR SC mode, while it is used for Y signal in the HETERO color mode. IC14 and 15, D/A converters, are used for R-Y and B-Y signals respectively in the HETERO color mode. Latches buffer the input data before each D/A conversion in each case.

Composite blanking is supplied to IC13 D/A converter, and a pedestal is generated with a fixed level during the blanking interval.

VIDEO PROCESSING
(REF. SCHEMATIC A2-3446)

In the VTR SC mode, the converted analog video signal is level-adjusted, amplified by Q40 - Q42, then goes to output amplifier.

In the HETERO color mode, the color difference component signals must be modulated on a subcarrier to create a composite color video signal. The Y signal is low pass filtered (L16, 17; C109 to C114), phase equalized (Q37 and Q38) and amplified before going to the output amplifier.

The R-Y and B-Y signals are passed through filters (L20, 21; C120 to C122) and L22, 23; C134 to C136), and amplified by Q44, Q48, Q51 and Q53. They are then clamped and connected to the modulator.

The modulation carriers are phase-shifted by IC12S (SYSTEM PHASE). They are additionally phase-shifted by IC11S and IC6E (CHROMA PHASE). One signal is supplied to modulator IC20 as the R-Y subcarrier. Another signal is delayed 90° and supplied to modulator IC18 as the B-Y subcarrier. The two modulated color signals are added, then amplified by Q46, Q47 and Q49 and supplied to IC21 where blanking is performed and burst is added.

When a MONOCHROME signal is supplied in the VTR SC mode, the chroma signal path is open-circuited by IC19.

Subcarrier which has been system-phased is supplied to the burst modulator IC24 and becomes burst signal at IC22-pin 13.

The burst flag signal to the burst modulator is shaped into a trapezoidal pulse by the filter which follows Q62, and is supplied to IC24 to gate on the burst subcarrier. It is then amplified by Q63. This burst signal is also added to sync in the Black Burst circuit which is composed at Q65 - Q68. The outputs (2) of this circuit appear at the rear panel at a level of 0.45 Vpp into 75 ohms. In the circuit centered around IC21, the blanking signal supplied to pins 2 and 6 switches between chroma and burst. Burst is therefore added to the chroma signal and they are amplified by Q54 and Q55. This signal is supplied to Video Output Amplifier. In the MONOCHROME mode, burst is eliminated by IC22.

SECTION 5

MAINTENANCE

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5-1. GENERAL

This section presents the basic information to maintain the equipment in the event of a failure. The information is presented in a table of circuit test points and notes which can also be used as an alignment procedure. In order to simplify the table, abbreviations are used as follows:

For transistors: E (Emitter), C (Collector), B (Base)
For FETs: G (Gain), D (Drain), S (Source)

Example: Q15-E (Transistor Q15 Emitter)
Example: Q21-G (FET Q21 Gate)

ICs and their pin-numbers are sometimes used as a Test Point;

Example: IC31-8 (IC31 pin 8)

Use of the following measurement equipment, or equivalent, is recommended:

NTSC Test Signal Generator:	Tektronix 1410
Color Monitor:	Tektronics 670 HR with external sync
Waveform Monitor:	Tektronix 1480 RJ
Vectorscope:	Tektronix 520A
Oscilloscope:	Dual Channel, greater than 100 MHz
Digital Voltmeter:	better than 0.01 V accuracy
U-Matic VTR:	BVU-200, AU-700, CR-8200

5-2. POWER SUPPLY

Remove the top panel of the Power Supply. Measure the terminal voltage inside the unit by using the digital Voltmeter. Adjust to within the following specified limits, if necessary.

	TEST POINT	ADJUSTMENT	MEASUREMENT VALUE	REQUIREMENTS	REMARKS
1	+5V Term.	+5V ADJ	+5.00 to +5.05V		
2	+12V Term.	+12V ADJ	+12.00 to +12.08V		
3	-12V Term.	-12V ADJ	-12.00 to -12.08V	+12V should be set first	
4	REG 1	none	-6.00 ±0.25V		
5	REG 2	none	-5.00 ±0.25V		

5-3. FRONT PANEL (INSIDE PCB)

	TEST POINT	MODE	CONTROL	MEASUREMENT VALUE	REQUIREMENTS	REMARKS
1	J1-1	All	VR15 ✓	+2.8V DC	Set VR16 to the center	VIDEO PHASE Sub Control *
2	J1-1	All	VR16	+2.75 to+2.9V DC	Set VR16 to the center after adjustment	VIDEO PHASE
3	J1-3	HETERO or VTR SC	S 2	Low -HETERO High-VTR SC		Operation mode
4	J1-7	B/W or COLOR	SW 7	Low -B/W High-COLOR		Operation mode
5	J1-8	BYPASS or OPERATE	S 1	Low - BYPASS High-OPERATE		Operation mode

	TEST POINT	MODE	CONTROL	MEASUREMENT VALUE	REQUIREMENTS	REMARKS
6	J1-15	All		+5V DC		DC Power Supply
7	J2-1	All	VR 4	+2 to +9V DC		VTR SC Chroma Phase Sub Control* 1-180° range
8	J2-2	All	VR 1	-1.8V DC	Unity adjustment ** for SET UP (Control knob in)	SET UP preset position
9	J2-2	All	VR 2	-1.4 to -2.0V DC	Vary VR-3 Variable for SET UP (Control knob out)	Used to adjust SET UP variable range
10	J2-4	All	SW 1	Low 180°; High 0°	Used in VTR SC mode	VTR SC 180° SW
11	J2-5	All	VR 5	+8V DC - final adjustment with Vectorscope	Unity adjustment ** for CHROMA PHASE (Control knob in)	CHROMA PHASE preset position
12	J2-5	All	VR 6 VR 8	+6 to +8.8V DC	Vary VR-7 Variable for CHROMA PHASE (knob out)	Used to adjust CHROMA PHASE variable range
13	J2-6	All	VR 12 ✓	+4V DC	Unity adj.**f.VIDEO LEVEL (knob in)	VIDEO LEVEL preset pos.
14	J2-6	All	VR 13 ✓	+2.3 to +11V DC	Vary VR-14 Variable for VIDEO LEVEL (knob out)	VIDEO LEVEL variable
15	J2-7	All	VR 9	-0.6V DC	Unity adj.**for CHROMA LEVEL (knob in)	CHROMA LEVEL preset pos.
16	J2-7	All	VR 10	+8 to -10V DC	Vary VR-11 Variable for CHROMA LEVEL (knob out)	CHROMA LEVEL variable range

<table>
<tr><th></th><th>TEST POINT</th><th>MODE</th><th>CONTROL</th><th colspan="8">MEASUREMENT VALUE</th><th colspan="8">REQUIREMENTS</th><th>REMARKS</th></tr>
<tr><td>17</td><td>J2-10</td><td>All</td><td></td><td colspan="8">+12V DC</td><td colspan="8"></td><td>+12V Power Supply</td></tr>
<tr><td>18</td><td>J2-12</td><td>All</td><td></td><td colspan="8">-12V DC</td><td colspan="8"></td><td>-12V Power Supply</td></tr>
<tr><td>19</td><td>J3-1</td><td>DOC ON or OFF</td><td>SW 6</td><td colspan="8">Low - ON
High - OFF</td><td colspan="8"></td><td>DOC switch</td></tr>
<tr><td>20</td><td>J3-3</td><td>VTR SC or HETERO</td><td>S 2</td><td colspan="8">Low - HETERO
High - VTR SC</td><td colspan="8"></td><td>OPERATE mode</td></tr>
<tr><td></td><td></td><td>ADV SYNC</td><td>SW 9
8 pos.</td><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td colspan="8">Position</td><td><i>see Note 3</i></td></tr>
<tr><td>21</td><td>J4-1</td><td></td><td></td><td>G</td><td>G</td><td>G</td><td>G</td><td>G</td><td>G</td><td>G</td><td>G</td><td colspan="8">G = Ground</td><td></td></tr>
<tr><td>22</td><td>J4-2</td><td></td><td></td><td></td><td>L</td><td></td><td>L</td><td></td><td>L</td><td></td><td>L</td><td colspan="8"></td><td></td></tr>
<tr><td>23</td><td>J4-3</td><td></td><td></td><td></td><td></td><td>L</td><td>L</td><td></td><td></td><td>L</td><td>L</td><td colspan="8"></td><td></td></tr>
<tr><td>24</td><td>J4-3</td><td></td><td></td><td></td><td></td><td></td><td></td><td>L</td><td>L</td><td>L</td><td>L</td><td colspan="8"></td><td></td></tr>
<tr><td>25</td><td>J4-5</td><td>Genlock SC</td><td>SW 4</td><td colspan="8">Low - NORMAL
High-non standard</td><td colspan="8"></td><td></td></tr>
<tr><td></td><td></td><td>H PHASE</td><td>SW 8
16 pos.</td><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td>9</td><td>10</td><td>11</td><td>12</td><td>13</td><td>14</td><td>15</td><td><i>see Note 3</i></td></tr>
<tr><td>26</td><td>J4-6</td><td></td><td></td><td>G</td><td>G</td><td>G</td><td>G</td><td>G</td><td>G</td><td>G</td><td>G</td><td>G</td><td>G</td><td>G</td><td>G</td><td>G</td><td>G</td><td>G</td><td>G</td><td></td></tr>
<tr><td>27</td><td>J4-7</td><td></td><td></td><td></td><td>L</td><td></td><td>L</td><td></td><td>L</td><td></td><td>L</td><td></td><td>L</td><td></td><td>L</td><td></td><td>L</td><td></td><td>L</td><td></td></tr>
<tr><td>28</td><td>J4-8</td><td></td><td></td><td></td><td></td><td>L</td><td>L</td><td></td><td></td><td>L</td><td>L</td><td></td><td></td><td>L</td><td>L</td><td></td><td></td><td>L</td><td>L</td><td></td></tr>
<tr><td>29</td><td>J4-9</td><td></td><td></td><td></td><td></td><td></td><td></td><td>L</td><td>L</td><td>L</td><td>L</td><td></td><td></td><td></td><td></td><td>L</td><td>L</td><td>L</td><td>L</td><td></td></tr>
<tr><td>30</td><td>J4-10</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td></td></tr>
<tr><td>31</td><td>J5-1</td><td>CHROMA PHASE</td><td></td><td colspan="8"></td><td colspan="8">see J2-5
Item 12 + 13</td><td></td></tr>
<tr><td>32</td><td>J5-4</td><td>HETERO 180° SW</td><td>SW 2</td><td colspan="8">Low - 180°
High - 0°</td><td colspan="8"></td><td></td></tr>
<tr><td>33</td><td>J5-5</td><td>HETERO or VTR SC</td><td>S 2</td><td colspan="8">Low - HETERO
High - VTR SC</td><td colspan="8"></td><td>OPERATE mode</td></tr>
<tr><td>34</td><td>J5-6</td><td>B/W or COLOR</td><td>SW 7</td><td colspan="8">Low - B/W
High - COLOR</td><td colspan="8"></td><td>OPERATE mode</td></tr>
<tr><td>35</td><td>J5-7</td><td>DUB or NOR</td><td>SW 5</td><td colspan="8">Low - DUB
High - NOR</td><td colspan="8"></td><td>OPERATE mode</td></tr>
</table>

	TEST POINT	MODE	CONTROL	MEASUREMENT VALUE	REQUIREMENTS	REMARKS
36	J5-8	SC PHASE 180°	SW 3	Low - 0° High -180°		SUBCARRIER PHASE 180° SW
37	J5-9	V-LOCK or NV-LOCK	S 1	Low - V-LOCK High - NV-LOCK		OPERATE mode
38	J5-10	SC PHASE	VR 17	+6.1 to 8.9V DC		SUBCARRIER PHASE variable

NOTES:

* 1. *"Sub" refers to Controls which have affect on the given parameter such as range centering but are not the primary operating controls.*

** 2. *"Unity" refers to output relative to input levels or phase position.*

3. *Low logic state are Ground. Other positions are high logic states.*

5-4. INPUT PROCESSOR

Y/C PROCESSOR

	TEST POINT	MODE	CONTROL	MEASUREMENT VALUE	REQUIREMENTS	REMARKS
1	TP-1	All	VR 3	1.2Vpp positive-going sync (video inverted)	Preset position for VIDEO LEVEL control on Front Panel	EIA Color-Bars
2	TP-1	All	VR 4	4.5MHz ±0.3dB	Preset position for CHROMA LEVEL control on Front Panel	Sweep Test Signal
3	TP-10*	VTR SC	VR 2	-1.8Vppinverted video; sync tip 0.0V	Same as Item 1	EIA Color-Bars
4	TP-10*	VTR SC	VR 4	4.5MHz ±0.3dB	Same as Item 2	Sweep Test Signal
5	TP-10*	HETERO	VR 7	Video-1.8V inverted video; pedestal 0.0V	Same es Item 1	EIA Color-Bars

	TEST POINT	MODE	CONTROL	MEASUREMENT VALUE	REQUIREMENTS	REMARKS
6	TP-10*	HETERO	L7, L8, L9	2.7MHz -0.5dB	Same as Item 2	Sweep Test Signal
7	TP-5	HETERO	VC 1	Aprrox. +5V DC	Same as Item 2	EIA Color-Bars
8	TP-6	HETERO		0.5Vpp B-Y SC	Same as Item 2	EIA Color-Bars
9	TP-7	HETERO	VR 8 (phase adjust)	0.6Vpp R-Y SC	Same as Item 2	EIA Color-Bars
10	TP-8	HETERO	VR 25	Approx.17Vpp,3µs wide at position of burst signal	Same as Item 2	EIA Color-Bars
11	TP-9	HETERO		Approx. 6Vpp,20µs wide at front edge of sync tip	Same as Item 2	EIA Color-Bars
12	TP-3	HETERO	VR 9	1.2Vpp negative B-Y	Same as Item 2	EIA Color-Bars
13	TP-4	HETERO	VR 18	1.2Vpp negative R-Y	Same as Item 2	EIA Color-Bars
14	TP-10*	VTR SC	VR 1	Flat group delay	Same as Items 1 and 2	2T Pulse and Bar
15	TP-10*	HETERO	VR 5 VR 6	Flat group delay	Same as Items 1 and 2	2T Pulse and Bar

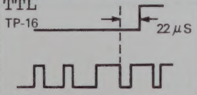
NOTE:
** 1: See A/D Converter Schematic A2-3489*

A/D CONVERTER

	TEST POINT	MODE	CONTROL	MEASUREMENT VALUE	REQUIREMENTS	REMARKS
1	TP-12	HETERO	VR 11 VR 12	4Vpp, 50% duty cycle	Preset for all the Controls on Front Panel	EIA Color-Bars
2	TP-13	HETERO	VR 11 VR 12	4Vpp, 50% duty cycle	Preset for all Controls on Front Pan.	EIA Color-Bars

	TEST POINT	MODE	CONTROL	MEASUREMENT VALUE	REQUIREMENTS	REMARKS
3	TP-14	HETERO	VR 13	TP-4 Pedestal Level	Preset for all Controls on Front Pan.	EIA Color-Bars
4	TP-11	HETERO	VR 15	Pedestal -1V	Preset for all Controls on Front Pan.	EIA Color-Bars
5	TP-11	VTR SC	VR 16	-0.5V DC	Preset for all Controls on Front Pan.	EIA Color-Bars
6	IC10-22	All	VR 17	-2V	Preset for all Controls on Front Pan.	EIA Color-Bars
7	IC8-4	All	VR 10	-0.42V DC	Preset for all Controls on Front Pan.	EIA Color-Bars

SYNC DETECTOR

	TEST POINT	MODE	CONTROL	MEASUREMENT VALUE	REQUIREMENTS	REMARKS
1	TP-15	All		Start Up Sync Output,TTL Level	Over entire range of VIDEO LEVEL on Front Panel	EIA Color-Bars
2	TP-17	All		Sync tip Level	Over entire range of VIDEO LEVEL on Front Panel	EIA Color-
3	TP-18	All		Pedestal Level	Over entire range of VIDEO LEVEL on Front Panel	EIA Color-Bars
4	TP-19	VTR SC		0.8Vpp inverted luminance signal pedestal -1V	Preset VIDEO LEVEL	EIA Color-Bars
5	TP-19	HETERO		1.2Vpp inverted luminance signal pedestal -0.75V	Preset VIDEO LEVEL	EIA Color-Bars
6	IC20-12	All	VR 24	Hetero -0.5V VTR SC -0.8V	Preset VIDEO LEVEL	EIA Color-Bars
7	TP-16 TP-19	All	VR 23	V Sync Output (at second seration) TTL 	Over entire range of VIDEO LEVEL on Front Panel	EIA Color-Bars

	TEST POINT	MODE	CONTROL	MEASUREMENT VALUE	REQUIREMENTS	REMARKS
8	TP-21	All	VR 27	Frame Pulse Field 1, TTL		EIA Color-Bars
9	Q77-C	All		17Vpp,at center of sync tip	Switching Pulse	EIA Color-Bars
10	Q76-C	All	VR 25	17Vpp, position of burst signal	Switching Pulse	EIA Color-Bars
11	IC5E-9	All		FLD ÷2, TTL		EIA Color-Bars
12	TP-10*	HETERO	VR 1 (Front Panel)	Pedestal 0	Preset SET UP	EIA Color-Bars
13	TP-10	VTR SC	VR 21	Sync tip 0	Preset SET UP	EIA Color-Bars
14	TP-10	VTR SC	VR 22	-0.7V DC	Preset SET UP	No signal input
15	LED Norm	All	VR 20, VR 19	Illumination of NORM LED	Preset VIDEO LEVEL	EIA Color-Bars
16	LED High	All	VR 20, VR 19	Illumination of HIGH LED	+2 dB VIDEO LEVEL	EIA Color-Bars
17	LED Low	All	VR 20, VR 19	Illumination of LOW LED	−2 dB VIDEO LEVEL	EIA Color-Bars

NOTE:
** 1: See A/D Converter As-3489*

INPUT VCO

	TEST POINT	MODE	CONTROL	MEASUREMENT VALUE	REQUIREMENTS	REMARKS
1	TP-44	All	VC 2	Check at V-rate so that sampling point is at the same level		EIA Color-Bars
2	TBC VIDEO OUT	HETERO	VR 30	Adjust for the same phase in BYPASS + OPERATE	Set VIDEO PHASE Control on Front Panel to center	EIA Color-Bars

	TEST POINT	MODE	CONTROL	MEASUREMENT VALUE	REQUIREMENTS	REMARKS
3	TBC VIDEO OUT	VTR SC	VR 32	Adjust for the same phase in BYPASS + OPERATE	Set VIDEO PHASE Control on Front Panel to center	EIA Color-Bars
4	TBC VIDEO OUT	NV-LOCK	VR 33	Same phase in BYPASS + OPERATE	Set VIDEO PHASE Control on Front Panel to center	EIA Color-Bars
5	4A-13	VTR SC	VR 35	Duty cycle 50%		EIA Color-Bars
6	VTR SC OUT	VTR SC	L 21	Good sine wave (min. harmonic distortion)		EIA Color-Bars
7	VTR SC OUT	VTR SC	VR 7 (Front Panel)	Over 180° range	Use a Vectorscope	EIA Color-Bars
8	VTR SC OUT	VTR SC	SW 1 (Front Panel)	180° phase change	Use a Vectorscope	EIA Color-Bars

FINAL OUTPUT AMPLIFIER

	TEST POINT	MODE	CONTROL	MEASUREMENT VALUE	REQUIREMENTS	REMARKS
1	VIDEO OUT 1 (VBS-1)	All	VR 38	Video 0.7Vpp	Preset for VIDEO LEVEL. Terminate VIDEO OUTPUT 2 (VBS 2) with 75Ω	EIA Color-Bars
2	VIDEO OUT 1	All	VR 39	Sync 0.3V	Preset for VIDEO LEVEL. Term. VIDEO OUT 2 with 75Ω	EIA Color-Bars
3	VIDEO OUT 1	VTR SC	VR 36	Flat group delay	Preset for VIDEO LEVEL. Term. VIDEO OUT 2 with 75Ω	2T Pulse and BAR
4	VIDEO OUT 1	VTR SC	VC 4	4.2MHz ±0.5dB	Preset for VIDEO LEVEL. Term. VIDEO OUT 2 with 75Ω	Sweep Test Signal

	TEST POINT	MODE	CONTROL	MEASUREMENT VALUE	REQUIREMENTS	REMARKS
5	VIDEO OUT 1	VTR SC	VR 40	Burst 0.3Vpp	Preset for VIDEO LEVEL. Term. VIDEO OUT 2 with 75Ω	EIA Color-BARS
6	NON-COMP (VB) OUT	All	VR 41	Video 0.7Vpp	Preset for VIDEO LEVEL	EIA Color-
7	NON-COMP OUT	VTR SC	VC 5	4.2MHz ±0.5dB	Preset for VIDEO LEVEL	Sweep Test Signal

5-5. MEMORY, MEMORY CONTROL, DOC

DOC

	TEST POINT	MODE	CONTROL	MEASUREMENT VALUE	REQUIREMENTS	REMARKS
1	TP-1	All		Normal +3.5V DC	Supply VTR RF signal to RF input	RF signal
2	TP-2	All	VR 1	Normal 1.5V DC	Supply VTR RF signal to RF input	RF signal
3	IC10P -13	All	SW 6 (Front Panel)	Low during operation; High during off		
4	IC8L-14	VTR SC		High		
5	IC8L-14	HETERO		Low		

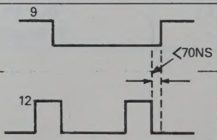
5-6. OUTPUT PROCESSOR

Set the VIDEO LEVEL, CHROMA LEVEL, CHROMA PHASE, and SET UP Controls to Preset position by pushing each control in. Also set the OPERATE/BYPASS switch to OPERATE.

On the Front Panel PCB, set the SW 4 Gen-Lock SC to the direction of the arrow, SW 5 NOR/DUB to NOR, and SW 7 COLOR/BW to COLOR.

Please note that the PCB alpha-numerics coordinates are given in parenthesis to assist in locating Test Points and adjustments.

	TEST POINT	MODE	CONTROL	MEASUREMENT VALUE	REQUIREMENTS	REMARKS
1			DSW 1 (9S)	Set 1,3 + 4 to OFF and 2 to ON.		
2	IC2-13	All		Sync 0.6Vpp; Sync tip at -0.5V		EIA Color-Bars
3	IC2-8 (8T)	All	VR 1 (7F)	Set the leading edge of V pulse to the center of 3rd seration		EIA Color-Bars
4	IC6H-5	All		2.5 µs positive going pulse		EIA Color-Bars
5	IC6H-4	All		40 to 50 µs negative going pulse		EIA Color-Bars
6	IC4J-1	All		40 to 50 µs Pulse blanking during V pulse interval		EIA Color-Bars
7	TP-1 (12F)	All	L6 (12F)	Adjust for maximum burst level		EIA Color-Bars
8	Q6-E (12F)	All	VR2 (6E)	Burst Flag should occur from the first cycle of burst		EIA Color-Bars
9	IC1-1 (11F)	All		Approx. 1.3Vpp 3.58MHz sine		EIA Color-Bars
10	IC8-14 (8J)	All		DC +6.3 to +7.7V (Regulator output)		EIA Color-Bars

	TEST POINT	MODE	CONTROL	MEASUREMENT VALUE	REQUIREMENTS	REMARKS
11	IC10-14 (12J)	All		DC +6.3 to +7.7V (Regulator Output)		EIA Color-Bars
12			VR 7 (9M)	Set to clockwise in maximum		
13	TP-3 (7M)	V-LOCK or EX.SYNC	VC 1	DC level approx. +5V		EIA Color-Bars
14	TP-3 (7M)	V-LOCK or EX.SYNC	VR 6	Minimize pulse-noise in V sync interval		EIA Color-Bars
15	IC8-17 (8J)	V-LOCK or EX.SYNC		Negative polarity H pulse		EIA Color-Bars
16	IC8-19 (8J)	V-LOCK or EX.SYNC		Negative polarity V pulse		EIA Color-Bars
17	TP-18 (7H)	V-LOCK or EX.SYNC	L 12 (7H)	Level approx. +3.0V DC		EIA Color-Bars
18	VIDEO OUT 1 (VBS-1)	V-LOCK or EX.SYNC	H PHASE (Front Panel)	H Sync phase	Minimize phase difference between BYPASS and OPERATE modes	EIA Color-Bars
19	IC6F-5	V-LOCK or EX.SYNC	VR 26 (6H)	Duty cycle 50%		EIA Color-Bars
20	IC6E-13	V-LOCK, EX.SYNC or HETERO	VR 25 (6E)	Duty cycle 50%		EIA Color-Bars
21	IC6A-1	V-LOCK	VR 9 (3F)	H Blanking 10.5 µs		EIA Color-Bars
22	Q58-E (12D)	V-LOCK	L 24 (12D)	Maximum width		EIA Color-Bars
23	IC2P-9	V-LOCK		Phase check		EIA Color-Bars
24	IC2P-2	V-LOCK	C 29	Within70 ns of phase difference		EIA Color-Bars

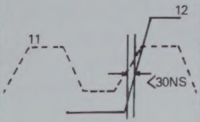
	TEST POINT	MODE	CONTROL	MEASUREMENT VALUE	REQUIREMENTS	REMARKS
25	IC13-4 DA		VR 14 (6A)	Level is -1.0V DC		EIA Color-Bars
26	TP7 (6A)	V-LOCK, HETERO		0.9 Vpp pedestal at -1.0V		EIA Color-Bars
27	TP7 (6A)	V-LOCK, VTR SC		Whith signal (peak) at -0.1V		EIA Color-Bars
28	TP8 (12A)	V-LOCK, HETERO		1.6Vpp luminance	Readjust INPUT PROCESSOR if there is a large difference when compared with 1.6Vpp	EIA Color-Bars
29	TP8 (12A)	V-LOCK, VTR SC	VR 11	1.6Vpp Comp Video		EIA Color-Bars
30	TP9 (8A)	V-LOCK, HETERO	VR 15 (INPUT PROC)	0.9Vpp, center is -0.5C DC.		EIA Color-Bars
31	TP11 (7A)	V-LOCK, HETERO	VR 8 (INPUT PROC)	Flatwave (-0.5V DC) when deleting B-Y		Full Color-Bars
32	TP11 (7A)	V-LOCK, HETERO	VR 11 (INPUT PROC)	Flatwave (-0.5V DC) during H Blanking interval	Turn on B-Y	Full Color-Bars
33	VIDEO OUT 1 (VBS-1)	V-LOCK, INT. SYNC, HETERO	VR 30 (INPUT PROC)	Match VIDEO PHASE in both BYPASS and OPERATE modes	Set VIDEO PHASE on Front Panel to the center position	EIA Color-Bars
34	VIDEO OUT 1	V-LOCK, INT. or EX.SYNC	VR 5 (9S)	Same VIDEO PHASE when Ref.Video is supplied or not		EIA Color-Bars
35	VIDEO OUT 1	V-LOCK INT. or EX.SYNC	H PHASE (Front Panel)	Reconfirm H PHASE	Readjust Item 18	EIA Color-Bars
36	VIDEO OUT 1	V-LOCK	VR 8 (3E)	Set Blanking Phase so no difference exists between BYPASS and OPERATE		Reverse Color-Bars

	TEST POINT	MODE	CONTROL	MEASUREMENT VALUE	REQUIREMENTS	REMARKS
37	VIDEO OUT 1	V-LOCK	VR 9 (3E)	Set Blanking Width so no difference exists between BYPASS and OPERATE		Reverse Color-Bars
38	VIDEO OUT 1	All	VR 27 (10D)	Minimize subcarrier leakage during H Blanking period		EIA Color-Bars
39	BLACK BURST 1 (BB 1)	All	VR 28 (7D)	Sync level >0.3 Vpp; Burst level 0.3Vpp	Terminate with 75Ω	EIA Color-Bars
40	VIDEO OUT 1	All	VR 19 (11C)	Burst level 0.3 Vpp		EIA Color-Bars
41	VIDEO OUT 1	All	L 28 (9D)	Burst waveform should be optimized	Vectorscope	EIA Color-Bars
42	VIDEO OUT 1	V-LOCK, INT. SYNC	VC 2 (10K)	Adjust for 3.579545MHz ±5Hz. *(see NOTE 1 on this page)*	When not adjustable set variation at TP3 in Item 13 to 4.5V, then readjust	EIA Color-Bars
43	VIDEO OUT 1	V-LOCK, EX.SYNC	SC PHASE (Front Panel)	Over 180° of variable range. Over 360° when used with SC PHASE 180° SW on Front Panel PCB	Vectorscope	EIA Color-Bars
44	VIDEO OUT 1	V-LOCK (Gen-Lock)	SC PHASE (Front Panel)	Set the same System Phase in BYPASS and OPERATE	Vectorscope	EIA Color-Bars
45	VIDEO OUT 1	HETERO	VR 24 (6E)	Set CHROMA PHASE to specified value	Use SW2 on Front Panel PCB if necessary	EIA Color-Bars

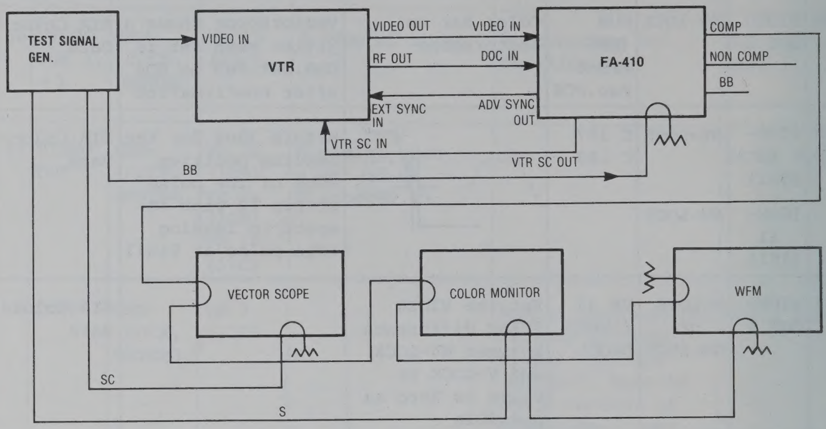
NOTE 1: A well-calibrated Sync Generator and Vecorscope can be used. Reference the Vectorscope to Sync Generator Subcarrier and view the TBC Color Bar output. Minimize vector rotation speed.

	TEST POINT	MODE	CONTROL	MEASUREMENT VALUE	REQUIREMENTS	REMARKS
46	VIDEO OUT 1	HETERO	VR 15 (11B) VR 16 (8C)	Match a center of vector	Set gain of Vectorscope in max.	EIA Color-Bars
47	VIDEO OUT 1	HETERO	VR 24 (6E)	Same PHASE R-Y signal with Burst	Set B-Y to OFF	Full Color-Bars
48	VIDEO OUT 1	HETERO	VC 5 (12D)	Set B-Y signal perpendicular to Burst	Set R-Y to OFF	Full Color-Bars
49	VIDEO OUT 1	HETERO	VR 23 (12C)	Chroma Level	Confirm frequency characteristics at Input and Output Processor with a Vectorscope	EIA Color-Bars
50	VIDEO OUT 1	HETERO	VR 17 (9C)	Chroma Level for B-Y direction	Confirm frequency characteristics at In-+ Output Proc. with Vectorscope	EIA Color-Bars
51	VIDEO OUT 1	HETERO	CHROMA PHASE (Front Panel)	Over 180°	Over 360°. Use with SW2 on Front Panel PCB	EIA Color-Bars
52	VIDEO OUT 1	GEN-LOCK	VR 32 (Input Proc)	Set VIDEO PHASE difference in HETERO and VTR SC to "O"		EIA Color-Bars
53	VIDEO OUT 1 NON - COMP	GEN-LOCK	VR 11 (7A)	Set VIDEO LEVEL difference in HETERO and VTR SC to "O"	Confirm if SET UP in Input Processor is correct	EIA Color-Bars
54	TP-12	GEN-LOCK, HETERO	VR 23 (12C)	2.0Vpp		EIA Color-Bars
55	VIDEO OUT 1, VIDEO OUT 3	GEN-LOCK	CHROMA LEVEL (Input Proc; Final Output Proc)	Specified value	Vectorscope	EIA Color-Bars

	TEST POINT	MODE	CONTROL	MEASUREMENT VALUE	REQUIREMENTS	REMARKS
56	VIDEO OUT 1, -3	GEN-LOCK, HETERO	VR 19 (11C)	0.3Vpp of Burst	Vectorscope and Oscilloscope	EIA Color-Bars
57	VIDEO OUT 1	GEN-LOCK, HETERO	VR 20 (10B) VR 21 (11B) VR 18 (11C)	Minimize transient of H Blanking		Black Burst
58	IC6P-5	GEN-LOCK, HETERO	VR 3 (12P)		Supply external reference to Test Signal Gen. and gen-lock. Turn SC PHASE control of Signal Gen., and confirm if high/low of TTL level is alternately varied proportionally	Black Burst
59	TP-5 (12H)	V-LOCK, EX.SYNC	L 14 (11J)	Approx. +3.0 V DC		EIA Color-Bars
60	TP-5 (12H)	NV-LOCK	VR 10 (10M)	Approx. +3.0 V DC	Set Waveform and Color Monitors to "Internal Sync"	EIA Color-Bars
61	TP-4 (8M)	NV-LOCK	L 11 (10J)	Approx. +3.0 V DC	Confirm correct picture is displayed on monitor in a range of +1 to 5.5VDC - allowing for appearance of vertical slipping	EIA Color-Bars
62	VIDEO OUT 1	NV-LOCK	VC 4 (12K)	See Item 42		EIA Color-Bars
63	VIDEO OUT 1	NV-LOCK		View Color Bars on Vectorscope	Set Vectorscope to Int. Sync and Burst Reference	EIA Color-Bars
64	VIDEO OUT 1	NV-LOCK	VR 10 (10M)	An 8H delay should be set relative to the VIDEO INPUT signal	Oscilloscope or Waveform Mon.	EIA Color-Bars

	TEST POINT	MODE	CONTROL	MEASUREMENT VALUE	REQUIREMENTS	REMARKS
65	VIDEO OUT 1	NV-LOCK	DUB (SW5 Front Pan.PCB	Color Bar on Vectorscope	Vectorscope shows a jitter when SW5 is DUB.Set SW5 to NOR after confirmation	EIA Color-Bars
66	IC3H-12 (3P1) IC3H-11 (1F1)	NV-LOCK NV-LOCK	C 187 C 189		Within 30ns for the leading positive edge of the pulse at Pin 12 with respect to leading edge pulse at Pin11	EIA Color-Bars
67	VIDEO OUT 1	V-LOCK or NV-LOCK	VR 33 (INPUT PROC)	Set the VIDEO PHASE difference between NV-LOCK and V-LOCK as close to Zero as possible		EIA Color-Bars
68	ADV SYNC	V-LOCK	Jumper JP 5	0.3Vpp 75Ω or 4.0Vpp 75Ω	Jumper plug: 2 Jumper plug: 1	EIA Color-Bars
69	ADV SYNC	V-LOCK	ADV. SYNC (Front Panel)	-8H compared to the Black Burst Output	Oscilloscope or Waveform Mon.	EIA Color-Bars
70	VIDEO OUT 1	All	DSW 2 DSW 3	Each H line from #10 to #20 can be blanked independently		EIA Color-Bars
71	VIDEO OUT 1	V-LOCK, HETERO	VR 13 (11A)	K Factor within 3%	Confirm K Factor of INPUT PROC at TP 10	2T Pulse and Bar

5-7. SYSTEM ALIGNMENT


TEST SIGNAL GEN.
VIDEO IN
VTR
VIDEO OUT
RF OUT
EXT SYNC IN
VTR SC IN
VIDEO IN
DOC IN
ADV SYNC OUT
FA-410
COMP
NON COMP
BB
VTR SC OUT
BB
VECTOR SCOPE
COLOR MONITOR
WFM
SC
S

	TEST POINT	MODE	CONTROL	MEASUREMENT VALUE	REQUIREMENTS	REMARKS
1	VIDEO OUT 1	V-LOCK	H PHASE (Front Panel)	Confirm Item 18 of Table for OUTPUT PROCESSOR		EIA Color-Bars
2	VIDEO OUT 1	V-LOCK	SC PHASE (F.Pan)	Confirm Item 44 of Table for OUTPUT PROCESSOR		EIA Color-Bars
3	VIDEO OUT 1	V-LOCK	VIDEO PHASE (F.Pan)	Set Video Phase difference in BYPASS and OPERATE to 0		EIA Color-Bars
4	VIDEO OUT 1	V-LOCK, EX.SYNC, HETERO	VR 5 (F.Pan PCB)	Set Color Bar to correct position on Vectorscope	Preset for CHROMA PHASE Control on Front Panel	EIA Color-Bars
5	VIDEO OUT 1	V-LOCK, EX.SYNC, VTR SC	VR 4 (F.Pan PCB)	Set Color Bar to correct position on Vectorscope	Preset for CHROMA PHASE Control on Front Panel	EIA Color-Bars
6	VIDEO OUT 1	V-LOCK, VTR SC	VR 16 (Input Proc)	Black clip substitution level, pedestal -0.015V	Confirmed by varying the SET UP Control	EIA Color-Bars

TEST POINT	MODE	CONTROL	MEASUREMENT VALUE	REQUIREMENTS	REMARKS
7 VIDEO OUT 1	V-LOCK VTR SC	VR 10 (Input Proc)	Black Clip threshold level, pedestal -0.03V	Confirmed by varying the SET UP Control	EIA Color-Bars
8 ADV SYNC	V-LOCK VTR SC	ADV SYNC (F.Pan)	-8H compared to Ext. Reference Input or TBC Output Sync	Confirm Item 69 of Table for OUTPUT PROCESSOR	EIA Color-Bars
9 VIDEO OUT 1	V-LOCK, HETERO		Correct phase on Vectorscope and Waveform Color Monitor	Replay recorded Color Bars	
10 VIDEO OUT 1	V-LOCK, VTR SC		Correct phase on Vectorscope and Waveform Color Monitor	Replay recorded Color Bars	
11 VIDEO OUT 1	NV-LOCK		Correct phase on Vectorscope and Waveform Color Monitor	Replay recorded Color Bars	
12 VIDEO OUT 1	V-LOCK, HETERO		Confirm DOC operation on monitor	Replay recorded Color Bars. Generation of guard band noise in shuttle, pause, etc.	
13 VIDEO OUT 1	V-LOCK, VTR SC		Confirm DOC operation on monitor	Replay recorded Color Bars. As above.	
14 VIDEO OUT 1	V-LOCK, MONO	SW 7 (F.Pan. PCB)	Confirm there is not Burst and the same bandwidth as in VTR SC mode exists. A Vectorscope, Waveform and Picture Mon. should be used.		EIA Color-Bars
15 VIDEO OUT 1	V-LOCK, HETERO	SW 2 (F.Pan. PCB)	Confirm 180° of phase shift on the Vectorscope		EIA Color-Bars
16 VIDEO OUT 1	V-LOCK, VTR SC	SW 1 F.Pan. PCB)	Confirm 180° of phase shift on the Vectorscope		EIA Color-Bars
17 VIDEO OUT 1	V-LOCK, VTR SC	SW 3 (F.P.)	Confirm 180° of System SC shift on the Vectorscope		EIA Color-Bars

NOTE 1: Set each respective switch to original position after adjustment for Items 14,15,16 and 17 of the above Table.

SECTION 6

SCHEMATICS

6-1. SCHEMATIC LIST....................6-1

6-1. SCHEMATIC LIST

This Section contains the Chassis Drawings, all Schematics for the FA-410 NTSC system as well as the pertaining Parts Lists.

TABLE 6-1. LIST OF SCHEMATICS

TITLE OF DRAWING	DRAWING NUMBER
EXTERNAL DIMENSIONS	FM2-821945
INPUT PROCESSOR BLOCK DIAGRAM	A2-3540
Y/C PROCESSOR	A2-3488
A/D CONVERTER	A2-3489
SYNC DETECTION	A2-3490
INPUT VCO	A2-3491
FINAL OUTPUT AMPLIFIER	A2-3492
MEMORY 1/2	A2-3409
MEMORY 2/2	A2-3410
MEMORY CONTROL	A2-3408
DOC	A2-3407
OUTPUT PROCESSOR BLOCK DIAGRAM	A2-3449
OUTPUT PROCESSOR 1/4	A2-3443
OUTPUT PROCESSOR 2/4	A2-3444
OUTPUT PROCESSOR 3/4	A2-3445
OUTPUT PROCESSOR 4/4	A2-3446

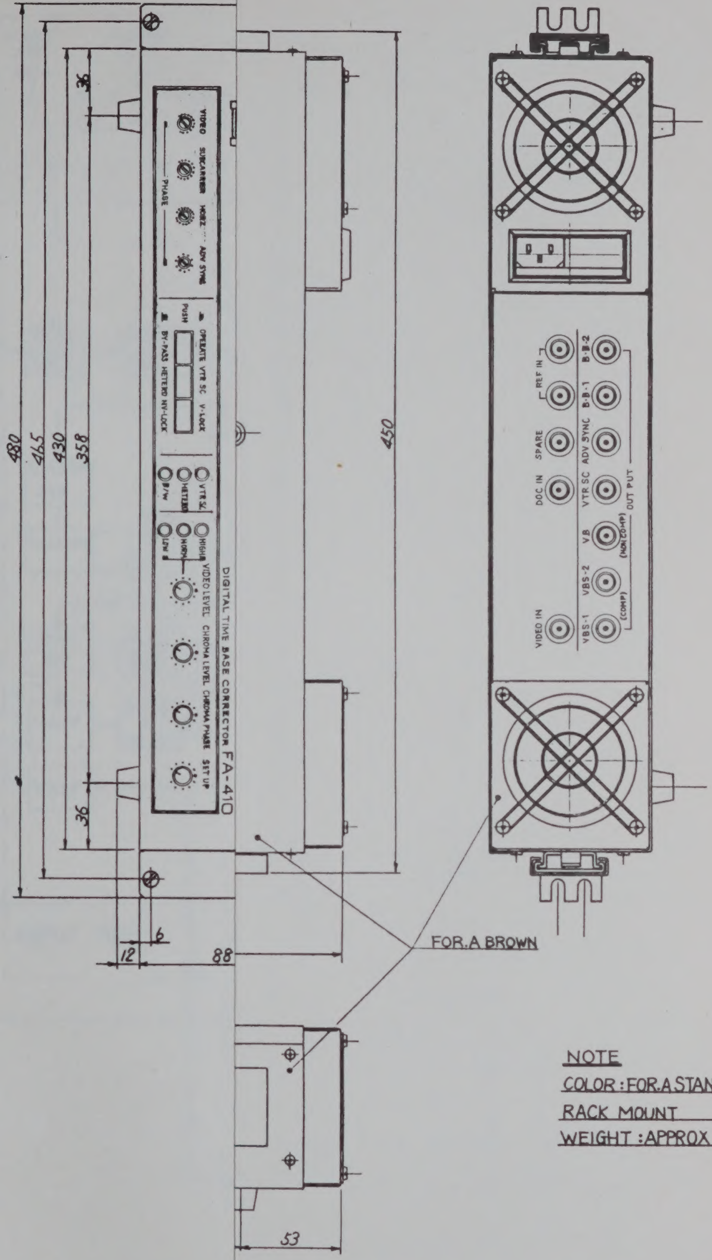
TABLE 6-1. LIST OF SCHEMATICS (Cont'd.)

TITLE OF DRAWING	DRAWING NUMBER
OPERATION PANEL 1/2	A3-2811
OPERATION PANEL 2/2	A2-3439
SWITCH PANEL	A4-2359
CONNECTOR BOARD	A2-3438
SYSTEM CONNECTION	A2-3541
POWER SUPPLY	A4-2361

Following Table 6-2 lists all abbreviations used in Section 5 and in the Schematics.

TABLE 6-2. LIST OF ABBREVIATIONS

ABBREVIATIONS	DEFINITION
R	Resistor
VR	Variable Resistor (Potentiometer)
C	Capacitor
VC	Variable Capacitor
L	Inductor
D	Diode
Q	Transistor or FET
IC	Integrated Circuit
RL	Relay
DL	Delay Line
S or SW	Switch
Y	Crystal
J	Jumper


480
465
430
358
36
36
450
6
12
88
53
VIDEO
SUBCARRIER
HORIZ
ADV SYNC
PHASE
OPERATE
VTR SC
V-LOCK
PUSH
BY-PASS
HETERO
HV-LOCK
VTR SC
HETERO
B/W
HIGH
NORM
LOW 8
VIDEO LEVEL
CHROMA LEVEL
CHROMA PHASE
SET UP
DIGITAL TIME BASE CORRECTOR FA-410
REF IN
B-B-2
B-B-1
SPARE
ADV SYNC
DOC IN
VTR SC
OUT PUT
VB
(NON COMP)
VBS-2
VIDEO IN
VBS-1
(COMP)
FOR.A BROWN

NOTE

COLOR : FOR.A STANDARD

RACK MOUNT

WEIGHT : APPROX Kg.

日附	材質	所要寸度	処理	~~クロメート~~ ~~塗装 焼付~~ ~~アルマイト~~
	設計	製図 中村 検図 承認	品名	FA-410 (NTSC) DIGITAL TIME BASE CORRECTOR
			名称	EXTERNAL DIMENSIONS
	尺度 1/2	個数 発行 57. 8. 12	図番	FM2-821945

TABLE 6-1. LIST OF SCHEMATICS (Cont'd.)

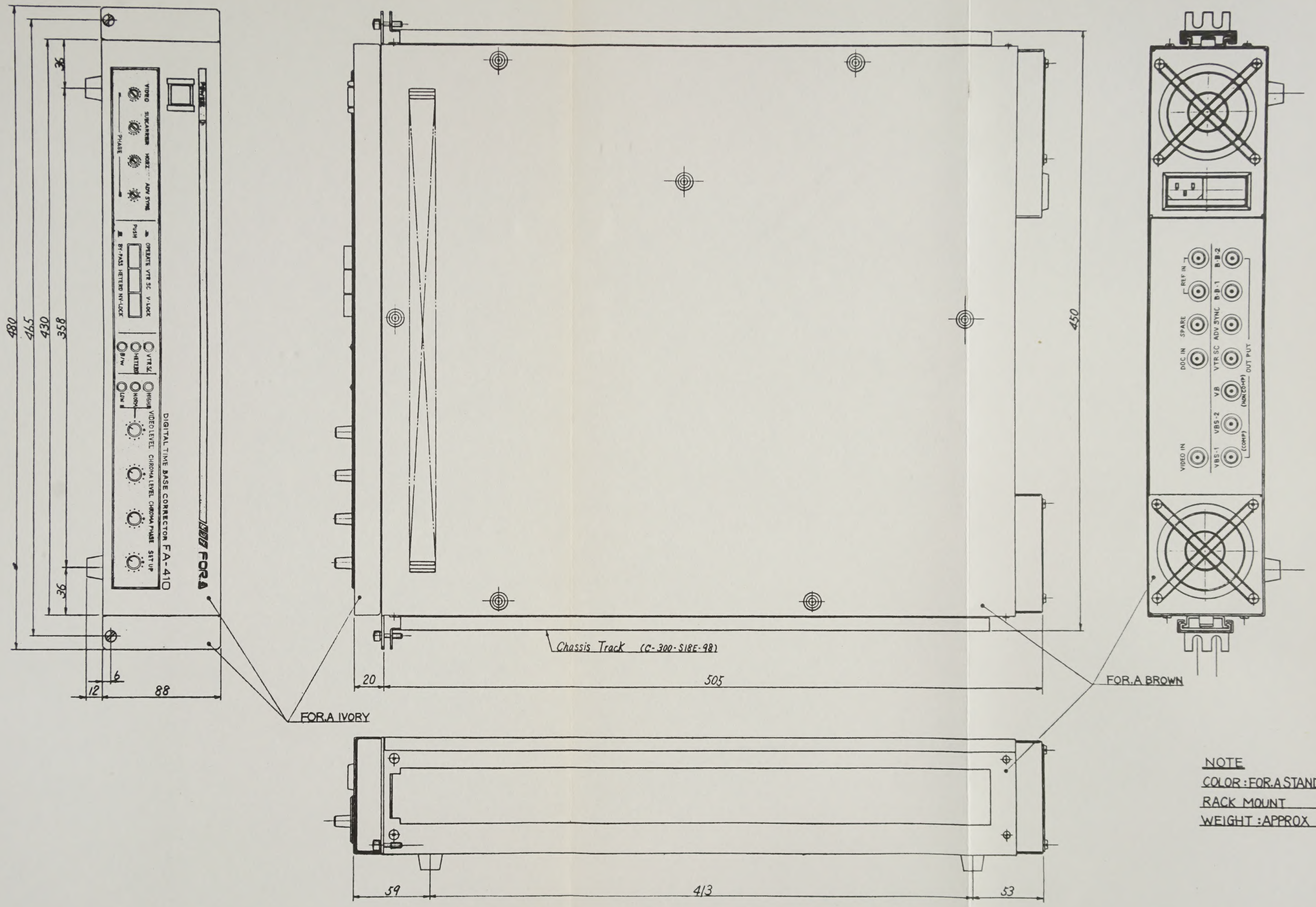
TITLE OF DRAWING	DRAWING NUMBER
OPERATION PANEL 1/2	A3-2811
OPERATION PANEL 2/2	A2-3439
SWITCH PANEL	A4-2359
CONNECTOR BOARD	A2-3438
SYSTEM CONNECTION	A2-3541
POWER SUPPLY	A4-2361

Following Table 6-2 lists all abbreviations used in Section 5 and in the Schematics.

TABLE 6-2. LIST OF ABBREVIATIONS

ABBREVIATIONS	DEFINITION
R	Resistor
VR	Variable Resistor (Potentiometer)
C	Capacitor
VC	Variable Capacitor
L	Inductor
D	Diode
Q	Transistor or FET
IC	Integrated Circuit
RL	Relay
DL	Delay Line
S or SW	Switch
Y	Crystal
J	Jumper

FM2-


480
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358
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36
12
6
88
VIDEO
SUBCARRIER
HORIZ
ADV SYNC
PHASE
OPERATE
VTR SC
V-LOCK
PUSH
BY-PASS
HETERO
NV-LOCK
VTR SC
HETERO
B/W
HIGH
NORM
LOW
VIDEO LEVEL
CHROMA LEVEL
CHROMA PHASE
SET UP
DIGITAL TIME BASE CORRECTOR FA-410
FOR.A
FOR.A IVORY
Chassis Track (C-300-S18E-98)
20
505
450
FOR.A BROWN
REF IN
B·B-2
B·B-1
SPARE
ADV SYNC
DOC IN
VTR SC
OUT PUT
VB
(NONCOMP)
VIDEO IN
VBS-2
VBS-1
(COMP)
59
413
53

NOTE

COLOR : FOR.A STANDARD

RACK MOUNT

WEIGHT : APPROX Kg.

改訂記事・日附	材質	所要寸度	処理	~~クロメート~~ ~~塗装・他上記~~ ~~アルマイト~~
	設計	製図 中村	検図 承認	品名名称	FA-410 (NTSC) DIGITAL TIME BASE CORRECTOR EXTERNAL DIMENSIONS
	尺度 1/2	個数 発行 57. 8. 12		図番	FM2-821945

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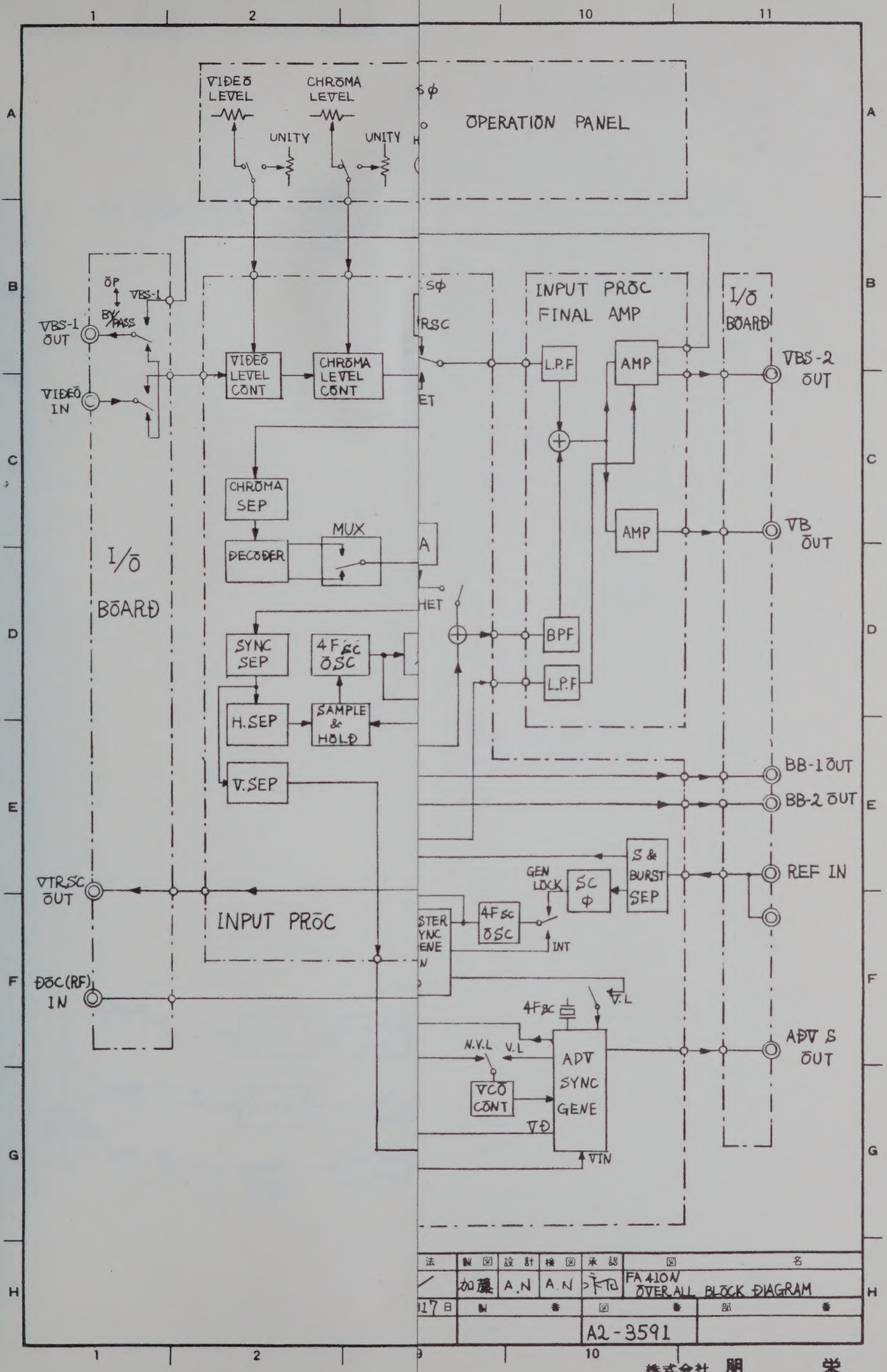
1
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A
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D
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G
H
VIDEO LEVEL
CHROMA LEVEL
UNITY
UNITY
Sφ
OPERATION PANEL
OP
BY PASS
VBS-1
VBS-1 OUT
VIDEO IN
I/O BOARD
VIDEO LEVEL CONT
CHROMA LEVEL CONT
Sφ
RSC
ET
INPUT PROC FINAL AMP
L.P.F
AMP
AMP
I/O BOARD
VBS-2 OUT
VB OUT
CHROMA SEP
DECODER
MUX
A
HET
BPF
L.P.F
SYNC SEP
4Fsc OSC
H.SEP
SAMPLE & HOLD
V.SEP
BB-1 OUT
BB-2 OUT
S & BURST SEP
REF IN
GEN LOCK
SC φ
INT
VTRSC OUT
INPUT PROC
STER YNC ENE N
4Fsc OSC
OSC(RF) IN
V.L
4Fsc
N.V.L
V.L
ADV SYNC GENE
ADV S OUT
VCO CONT
VD
VIN

法	製図	設計	検図	承認	図 名
／	加藤	A.N	A.N	永田	FA 410N OVER ALL BLOCK DIAGRAM
17日	製 番		図 番	部 番	
			A2-3591		

株式会社 朋 栄

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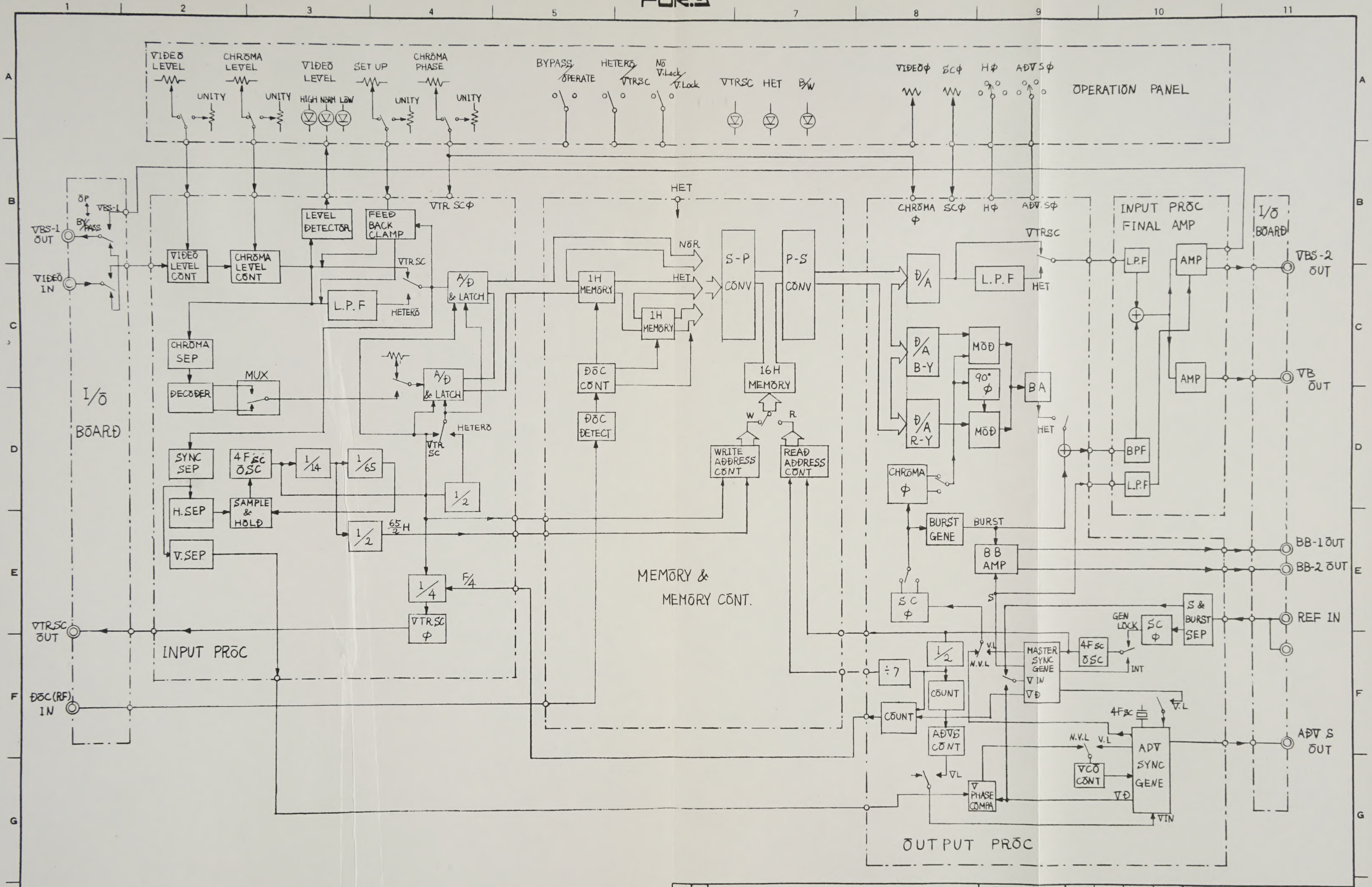
OPERATION PANEL
VIDEO LEVEL
CHROMA LEVEL
VIDEO LEVEL
SET UP
CHROMA PHASE
UNITY
HIGH NORM LOW
BYPASS / OPERATE
HETERO / VTRSC
No V.Lock / V.Lock
VTRSC HET B/W
VIDEO φ SC φ H φ ADV S φ
I/O BOARD
OP
BY PASS
VBS-1
VBS-1 OUT
VIDEO IN
VTRSC OUT
DOC(RF) IN
VIDEO LEVEL CONT
CHROMA LEVEL CONT
LEVEL DETECTOR
FEED BACK CLAMP
VTR SC φ
VTR.SC
L.P.F
HETERO
A/D & LATCH
CHROMA SEP
DECODER
MUX
SYNC SEP
4Fsc OSC
1/14
1/65
1/2
H.SEP
SAMPLE & HOLD
65/2 H
V.SEP
1/4
F/4
VTR.SC φ
INPUT PROC
HET
NOR
1H MEMORY
S-P CONV
P-S CONV
16H MEMORY
W
R
WRITE ADDRESS CONT
READ ADDRESS CONT
DOC CONT
DOC DETECT
MEMORY & MEMORY CONT.
CHROMA φ
SC φ
H φ
ADV.S φ
VTRSC
D/A
L.P.F
D/A B-Y
D/A R-Y
MOD
90° φ
BA
CHROMA φ
BURST GENE
BURST
BB AMP
SC φ
S
INPUT PROC FINAL AMP
BPF
AMP
VBS-2 OUT
VB OUT
BB-1 OUT
BB-2 OUT
REF IN
ADV S OUT
S & BURST SEP
GEN LOCK
SC φ
4Fsc OSC
INT
MASTER SYNC GENE
V.L
N.V.L
V IN
V D
÷7
COUNT
ADVS CONT
V PHASE COMPA
VCO CONT
4Fsc
ADV SYNC GENE
VIN
OUTPUT PROC

改訂	A

第三角図法	製図	設計	検図	承認	図名
尺度 /	加藤	A.N	A.N	永田	FA 410N OVERALL BLOCK DIAGRAM
作成58年5月17日	製番		図番	A2-3591	部番
個数					

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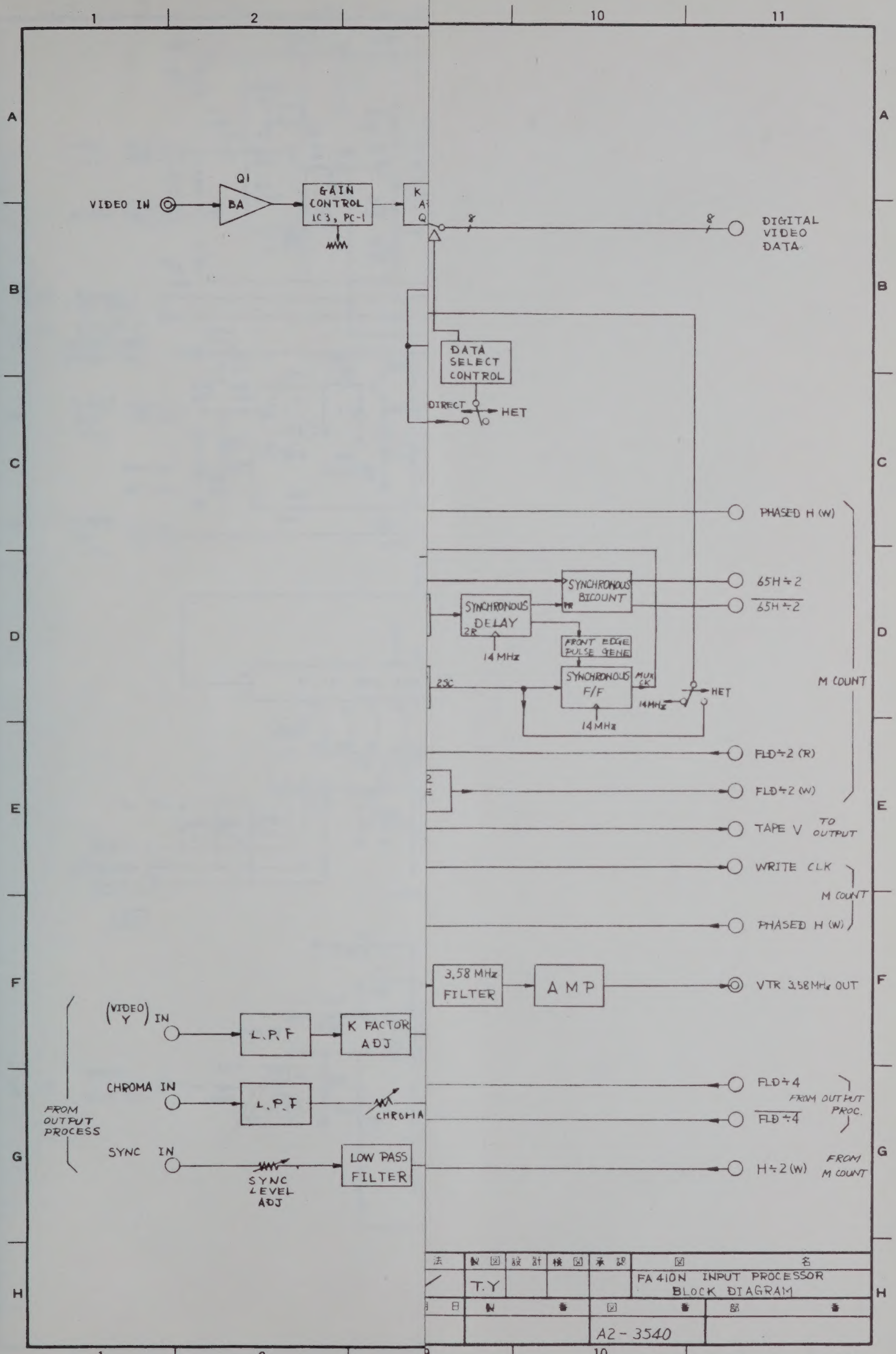
1
2
10
11
A
B
C
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F
G
H
VIDEO IN
Q1
BA
GAIN CONTROL IC3, PC-1
K
A
Q
8
8
DIGITAL VIDEO DATA
DATA SELECT CONTROL
DIRECT
HET
PHASED H (W)
65H ÷ 2
$\overline{65H \div 2}$
SYNCHRONOUS BICOUNT
SYNCHRONOUS DELAY
2R
14 MHz
FRONT EDGE PULSE GENE
SYNCHRONOUS F/F
MUX CK
2SC
14MHz
HET
14MHz
M COUNT
FLD÷2 (R)
FLD÷2 (W)
TAPE V
TO OUTPUT
WRITE CLK
M COUNT
PHASED H (W)
3.58 MHz FILTER
AMP
VTR 3.58MHz OUT
(VIDEO Y) IN
L.P.F
K FACTOR ADJ
CHROMA IN
L.P.F
CHROMA
FROM OUTPUT PROCESS
SYNC IN
SYNC LEVEL ADJ
LOW PASS FILTER
FLD÷4
$\overline{FLD \div 4}$
FROM OUTPUT PROC.
H÷2(W)
FROM M COUNT

法	製図	設計	検図	承認	図名
	T.Y				FA410N INPUT PROCESSOR BLOCK DIAGRAM

日	製番	図番	部番
		A2-3540	

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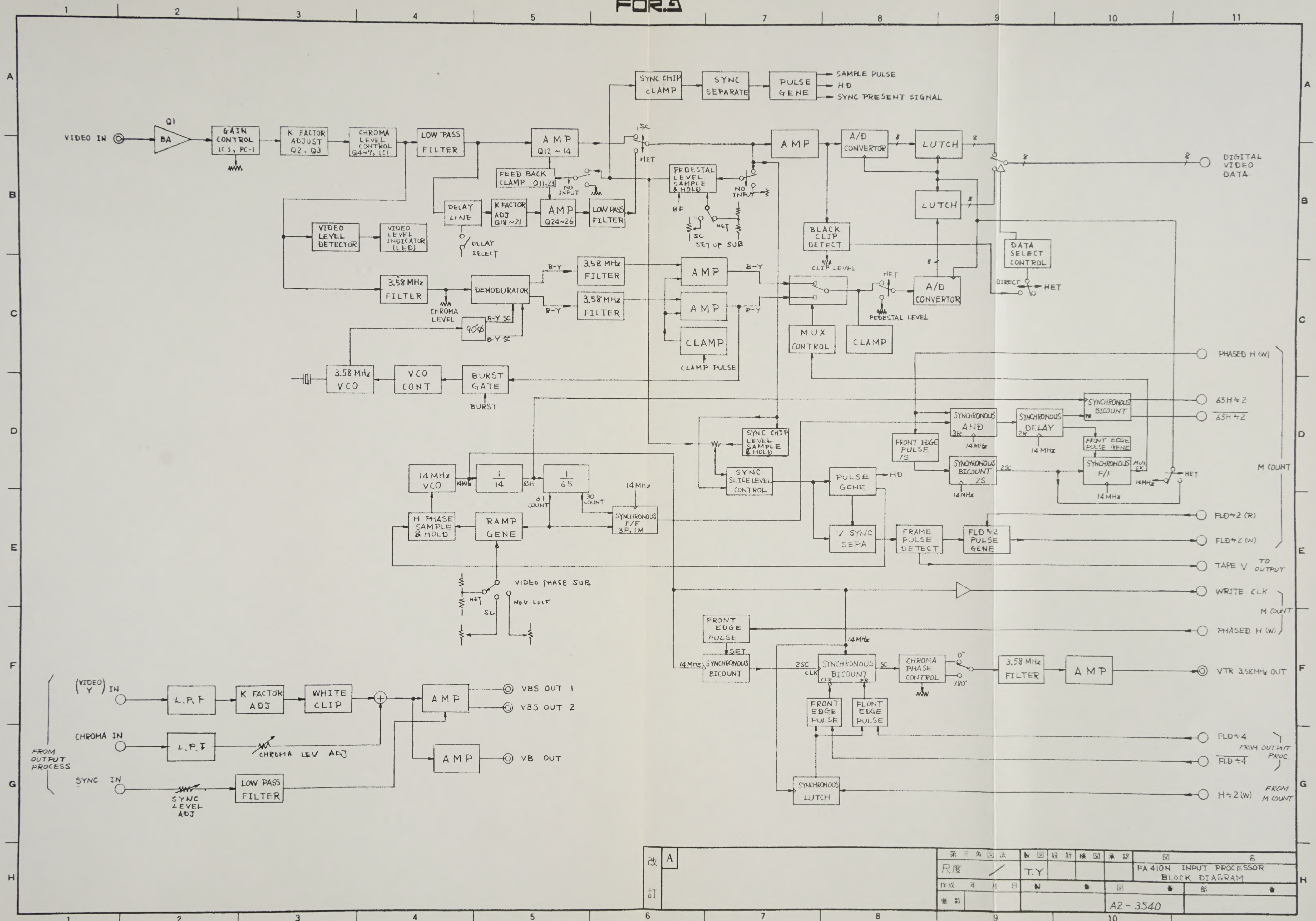
FOR.A


VIDEO IN
Q1
BA
GAIN CONTROL IC3, PC-1
K FACTOR ADJUST Q2, Q3
CHROMA LEVEL CONTROL Q4~7, IC1
LOW PASS FILTER
AMP Q12 ~ 14
SYNC CHIP CLAMP
SYNC SEPARATE
PULSE GENE
SAMPLE PULSE
HD
SYNC PRESENT SIGNAL
SC
HET
FEED BACK CLAMP Q11, 23
NO INPUT
PEDESTAL LEVEL SAMPLE & HOLD
BF
SC
HET
SET UP SUB
AMP
A/D CONVERTOR
8
LUTCH
LUTCH
DIGITAL VIDEO DATA
DELAY LINE
K FACTOR ADJ Q18~21
AMP Q24~26
LOW PASS FILTER
DELAY SELECT
VIDEO LEVEL DETECTOR
VIDEO LEVEL INDICATOR (LED)
BLACK CLIP DETECT
CLIP LEVEL
DATA SELECT CONTROL
DIRECT
HET
3.58MHz FILTER
DEMODURATOR
CHROMA LEVEL
B-Y
R-Y
3.58MHz FILTER
3.58MHz FILTER
AMP
AMP
CLAMP
CLAMP PULSE
MUX CONTROL
CLAMP
A/D CONVERTOR
PEDESTAL LEVEL
90°
R-Y SC
B-Y SC
3.58MHz VCO
VCO CONT
BURST GATE
BURST
PHASED H (W)
65H÷2
65H÷2
SYNCHRONOUS BICOUNT
SYNCHRONOUS AND
SYNCHRONOUS DELAY
3R
2R
14MHz
FRONT EDGE PULSE 1S
FRONT EDGE PULSE GENE
SYNCHRONOUS BICOUNT 2S
2SC
SYNCHRONOUS F/F
MUX CLK
M COUNT
14MHz VCO
1/14
1/65
65H
61 COUNT
30 COUNT
SYNC CHIP LEVEL SAMPLE & HOLD
SYNC SLICE LEVEL CONTROL
PULSE GENE
HD
V SYNC SEPA
FRAME PULSE DETECT
FLD÷2 PULSE GENE
FLD÷2 (R)
FLD÷2 (W)
TAPE V
TO OUTPUT
WRITE CLK
H PHASE SAMPLE & HOLD
RAMP GENE
SYNCHRONOUS F/F 3P, 1M
VIDEO PHASE SUB
HET
SC
NOV. LOCK
FRONT EDGE PULSE
SET
SYNCHRONOUS BICOUNT
SYNCHRONOUS BICOUNT
CLK
CLR
PR
CHROMA PHASE CONTROL
0°
180°
3.58MHz FILTER
AMP
VTR 3.58MHz OUT
FRONT EDGE PULSE
FRONT EDGE PULSE
FLD÷4
FLD÷4
FROM OUTPUT PROC.
SYNCHRONOUS LUTCH
H÷2 (W)
FROM M COUNT
(VIDEO Y) IN
L.P.F
K FACTOR ADJ
WHITE CLIP
AMP
VBS OUT 1
VBS OUT 2
CHROMA IN
L.P.F
CHROMA LEV ADJ
AMP
VB OUT
SYNC IN
SYNC LEVEL ADJ
LOW PASS FILTER
FROM OUTPUT PROCESS
1
2
3
4
5
6
7
8
9
10
11
A
B
C
D
E
F
G
H

改訂 A

第三角図法

尺度 /

製図 T.Y

設計

検図

承認

図名 FA 410N INPUT PROCESSOR BLOCK DIAGRAM

作成 年 月 日

製番

図番 A2-3540

部番

個数

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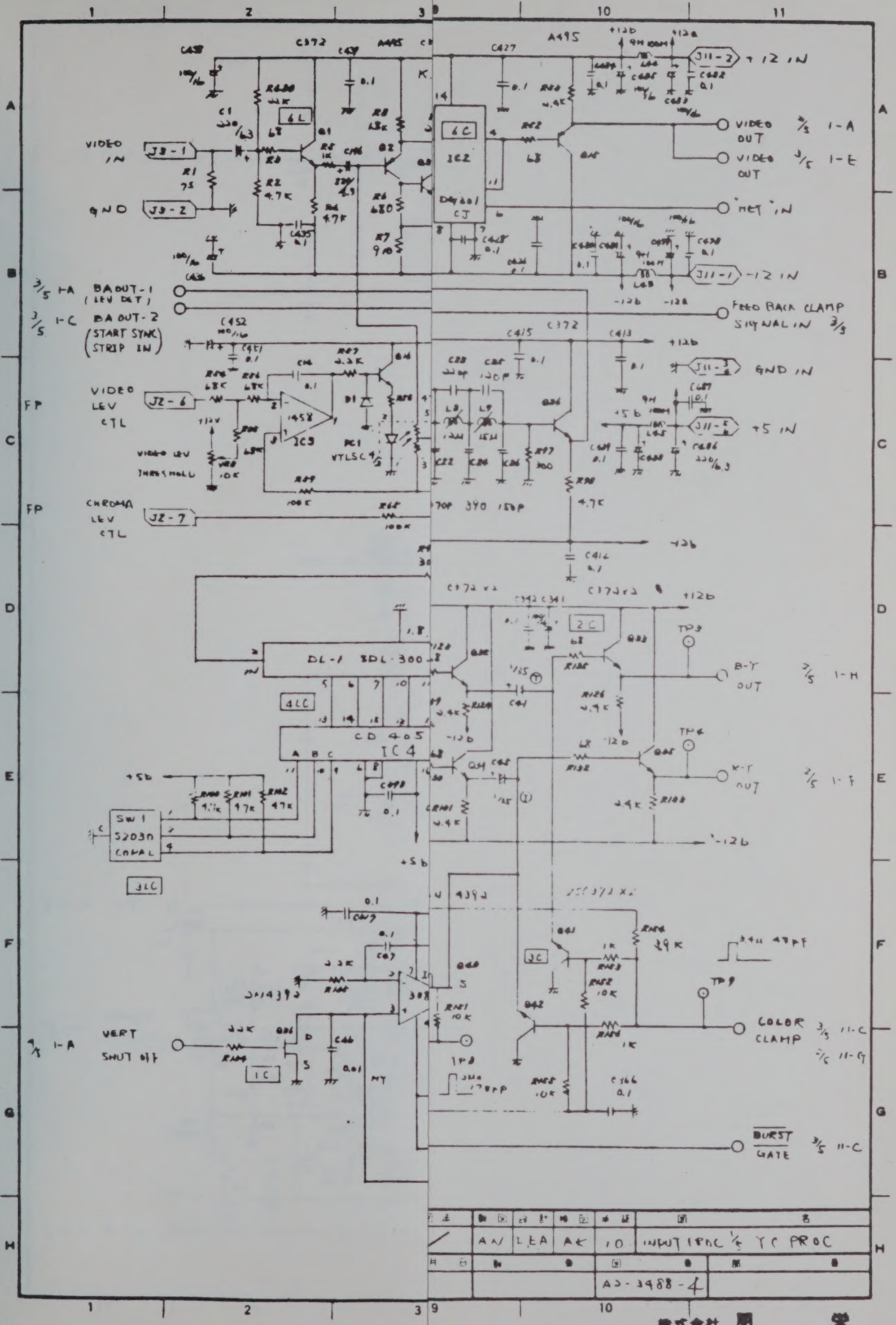
VIDEO IN
J3-1
GND
J3-2
R1 75
C1 220/6.3
R2 4.7K
R4 4.7K
Q1
Q2
R5 1K
R6 680
R7 910
R8 1.8K
C372
A495
C427
6L
6C
IC2
D4/301 CJ
R62 68
J11-2
+12 IN
+12b
+12a
VIDEO OUT 3/5 1-A
VIDEO OUT 3/5 1-E
"MET" IN
J11-1
-12 IN
-12b
-12a
BA OUT-1 (LEV DET) 3/5 1-A
BA OUT-2 (START SYNC STRIP IN) 3/5 1-C
FEED BACK CLAMP SIGNAL IN 3/5
C452
C415
C413
GND IN
J11-3
+5 IN
J11-5
+5b
FP
VIDEO LEV CTL
J2-6
1458
IC3
D1
PC1 VTL5C4/2
VIDEO LEV THRESHOLD
VR8 10K
R49 100K
CHROMA LEV CTL
J2-7
R65 100K
R97 300
R98 4.7K
120P
15M
C416 0.1
DL-1 3DL-300
4LC
CD 405
IC4
A B C
+5b
SW1 S203D COPAL
R100 4.7K
R101 47K
R102 47K
3LC
2C
TP3
B-Y OUT 3/5 1-H
TP4
R-Y OUT 3/5 1-F
R126 4.4K
R132
R133 4.4K
R128
-12b
0.1
C47
C87
2.2K
308
RN1 10K
TP8
VERT SHUT OFF 4/5 1-A
R149
1C
C46 0.01
Q41
Q42
3C
R143 1K
R152 10K
R148 29K
R146 1K
R155 10K
C166 0.1
TP9
3.4μ 47PF
COLOR CLAMP 3/5 11-C 5/5 11-G
BURST GATE 3/5 11-C
1 2 3 9 10 11
A B C D E F G H

AN	I.EA	AK	10	INPUT PROC 1/5 YC PROC
		AS-3488-4		

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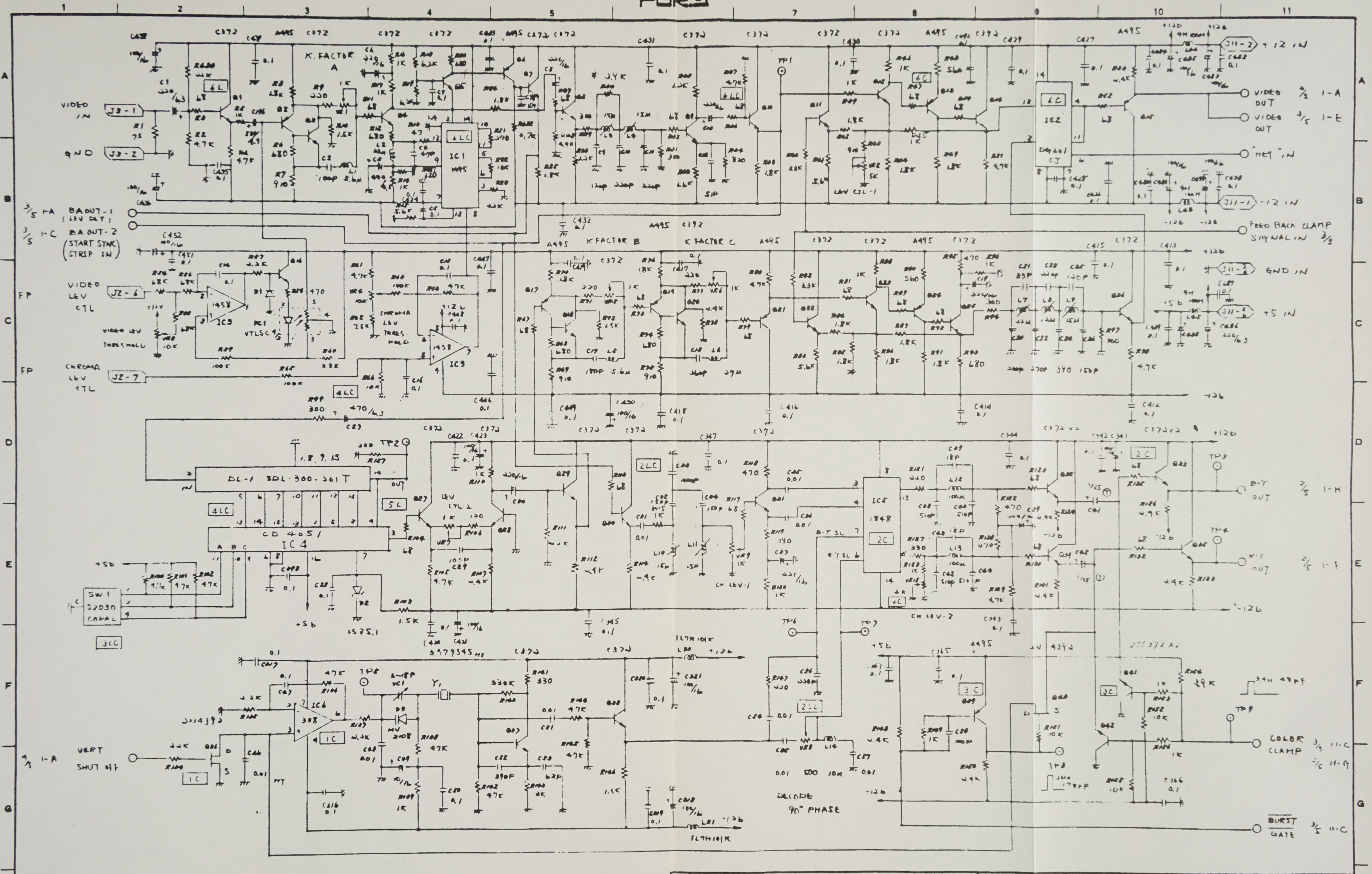
FOR.A



VIDEO IN J3-1
GND J3-2
K. FACTOR A
IC1 M495
6LC
IC2 D4401 CJ
6C
J11-2 +12 IN
VIDEO OUT 3/5 1-A
VIDEO OUT 3/5 1-E
"RET" IN
J11-1 -12 IN
FEED BACK CLAMP SIGNAL IN 3/5
3/5 1-A BA OUT-1 (LEV DET)
3/5 1-C BA OUT-2 (START SYNC STRIP IN)
FP VIDEO LEV CTL J2-6
IC3 1458
PC1 VTLSC 4/5
VIDEO LEV THRESHOLD
CHROMA LEV THRES. HOLD
FP CHROMA LEV CTL J2-7
4LC
K FACTOR B
K FACTOR C
J11-3 GND IN
J11-5 +5 IN
TP1
TP2
DL-1 SDL-300-201T
CD 4051 IC4
SW1 S203D CORAL
3LC
5L
LEV CTL-2
2LC
CH LEV-1
IC5 1848
2C
CH LEV-2
TP3
B-Y OUT 3/5 1-H
TP4
R-Y OUT 3/5 1-F
B-Y SL
R-Y SL
TP6
TP7
3579545 Hz
15.75.1
FL7H101K
IC6 308
1C
3/5 1-A VERT SHUT OFF
TP8
Y1
DECODE 90° PHASE
3C
TP9
COLOR CLAMP 3/5 11-C 2/5 11-G
BURST GATE 3/5 11-C

改	A	第三角図法	製図	設計	検図	承認	図名	
訂	TP 30~43 GND	尺度 /	AN	LEA	AK	10	INPUT PROC 1/5 Y C PROC	
		作成 年 月 日	製番		図番		部番	
		個数			A5-3488-4			

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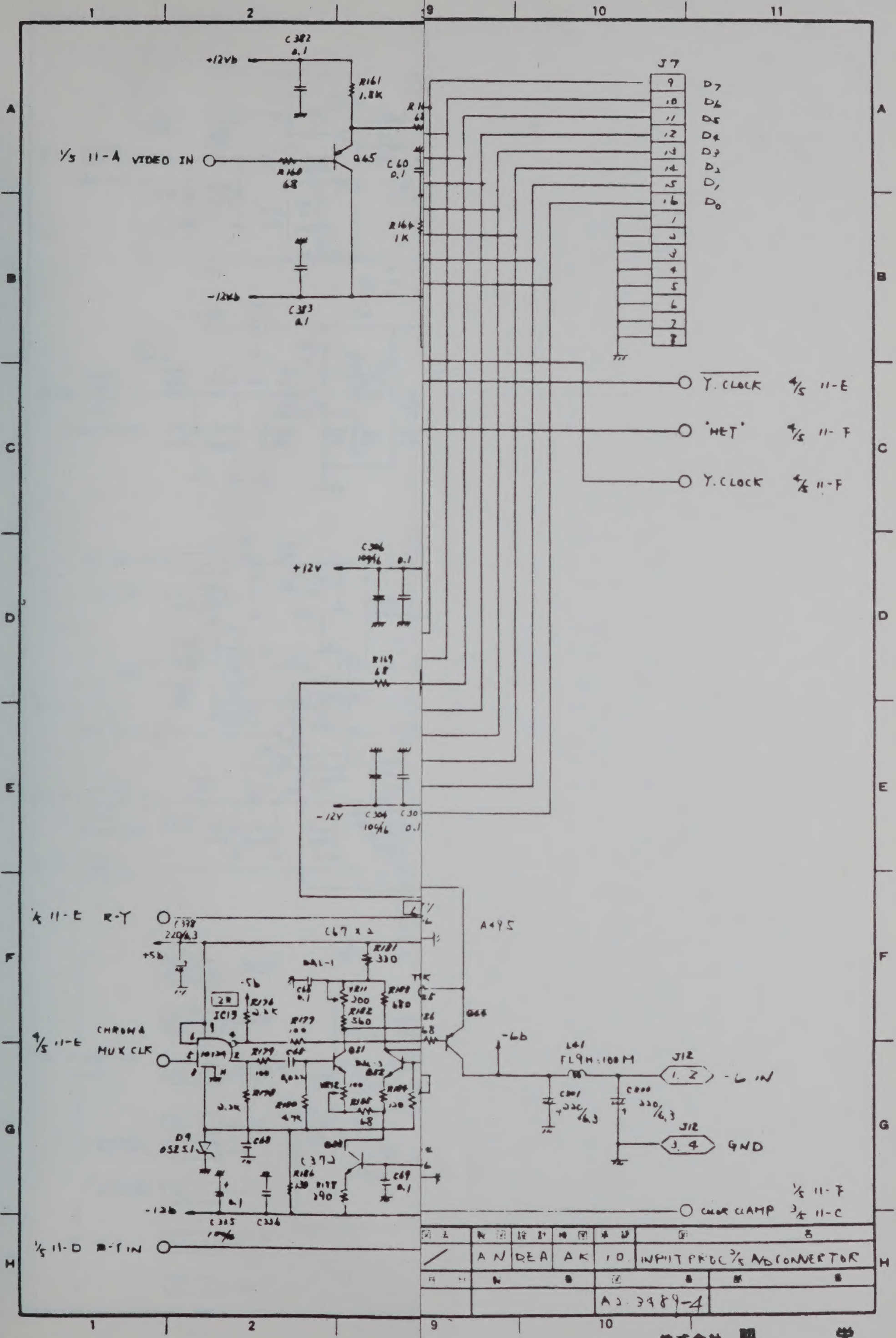

1
2
9
10
11
A
B
C
D
E
F
G
H
+12Vb
C382
0.1
R161
1.8K
R1
62
1/5 11-A VIDEO IN
R160
68
Q65
C60
0.1
R164
1K
-12Vb
C383
0.1
J7
9
10
11
12
13
14
15
16
1
2
3
4
5
6
7
8
D7
D6
D5
D4
D3
D2
D1
D0
Y. CLOCK 4/5 11-E
'HET' 4/5 11-F
Y. CLOCK 4/5 11-F
C306
10/16
0.1
+12V
R169
68
-12V
C304
10/16
C30
0.1
1/5 11-E R-Y
C378
220/6.3
+5b
C67 x 2
R181
330
BAL-1
A495
-5b
R176
2.2K
IC13
C66
0.1
VR11
200
R182
560
R183
680
1K
R177
100
68
Q64
4/5 11-E CHROMA MUX CLK
R179
100
Q51
Q52
-6b
L41
FL9H:100M
J12
1, 2
-6 IN
R178
2.2K
R180
4.7K
R185
68
R184
120
C301
330/6.3
C000
330/6.3
J12
3, 4
GND
D9
05Z5.1
C68
C372
R186
120
R178
390
C69
0.1
0.1
-12b
C305
10/16
C336
1/5 11-F
COLOR CLAMP 3/5 11-C
1/5 11-D B-Y IN
AN
DEA
AK
10.
INPUT PROC 3/5 A/D CONVERTOR
A2 3489-4

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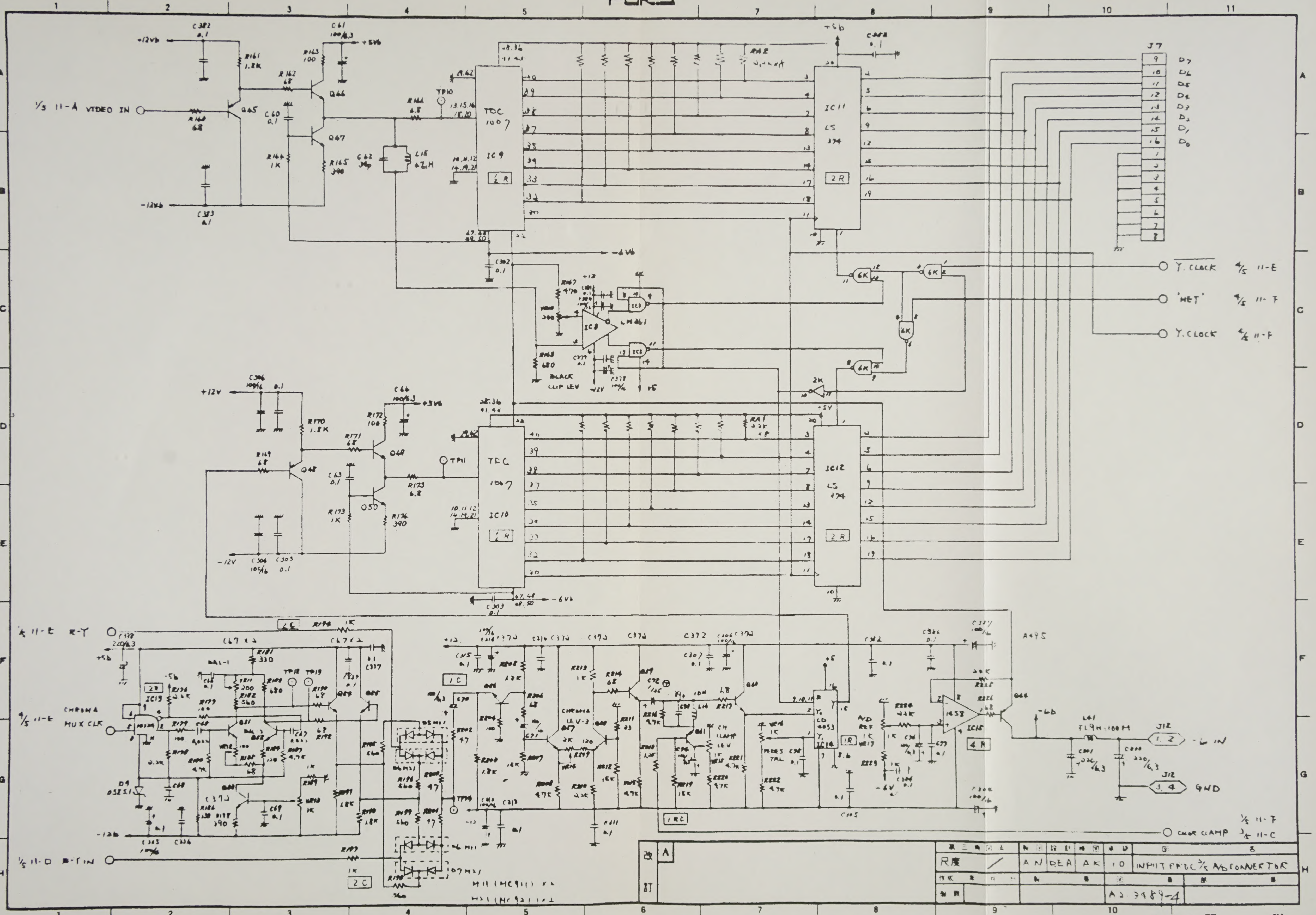
FOR.A



1/5 11-A VIDEO IN
+12Vb
-12Vb
Q65
Q66
Q67
R161 1.8K
R162 68
R163 100
R160 68
R164 1K
R165 390
R166 6.8
C60 0.1
C61 100/6.3
C62 34p
L15 6.2μH
C382 0.1
C383 0.1
TP10
TDC 1007 IC9
2R
IC11 LS 374
RA2
+5b
-6Vb
J7
D7
D6
D5
D4
D3
D2
D1
D0
Y. CLOCK 4/5 11-E
'HET' 4/5 11-F
Y. CLOCK 4/5 11-F
6K
2K
IC8 LM361
BLACK CLIP LEV
R167 470
R168 680
+12V
-12V
Q68
Q69
Q50
R169 68
R170 1.8K
R171 68
R172 100
R173 1K
R174 390
R175 6.8
C63 0.1
C64 100/6.3
C304 100/6
C305 0.1
C306 100/6
TP11
TDC 1007 IC10
IC12 LS 374
RA1
C303 0.1
1/5 11-E R-Y
4/5 11-E CHROMA MUX CLK
1/5 11-D B-Y IN
IC13
D9 05Z5.1
Q51
Q52
Q53
Q54
Q55
Q56
Q57
Q58
Q59
Q60
Q61
TP12
TP13
TP14
CHROMA LEV-3
CH CLAMP LEV
RES TAL
CD 4053 IC14
AD REF
1458 IC15
L41 FL9H:100M
J12 1.2 -C IN
J12 3.4 GND
COLOR CLAMP 1/5 11-F 3/5 11-C
M11 (MC911) ×2
M21 (MC921) ×2
1C
2C
1RC
1R
4R
A495
改訂 A
尺度
AN
DEA
AK
10
INPUT PROC 3/5 A/D CONVERTOR
作成
製図
A2-3489-4

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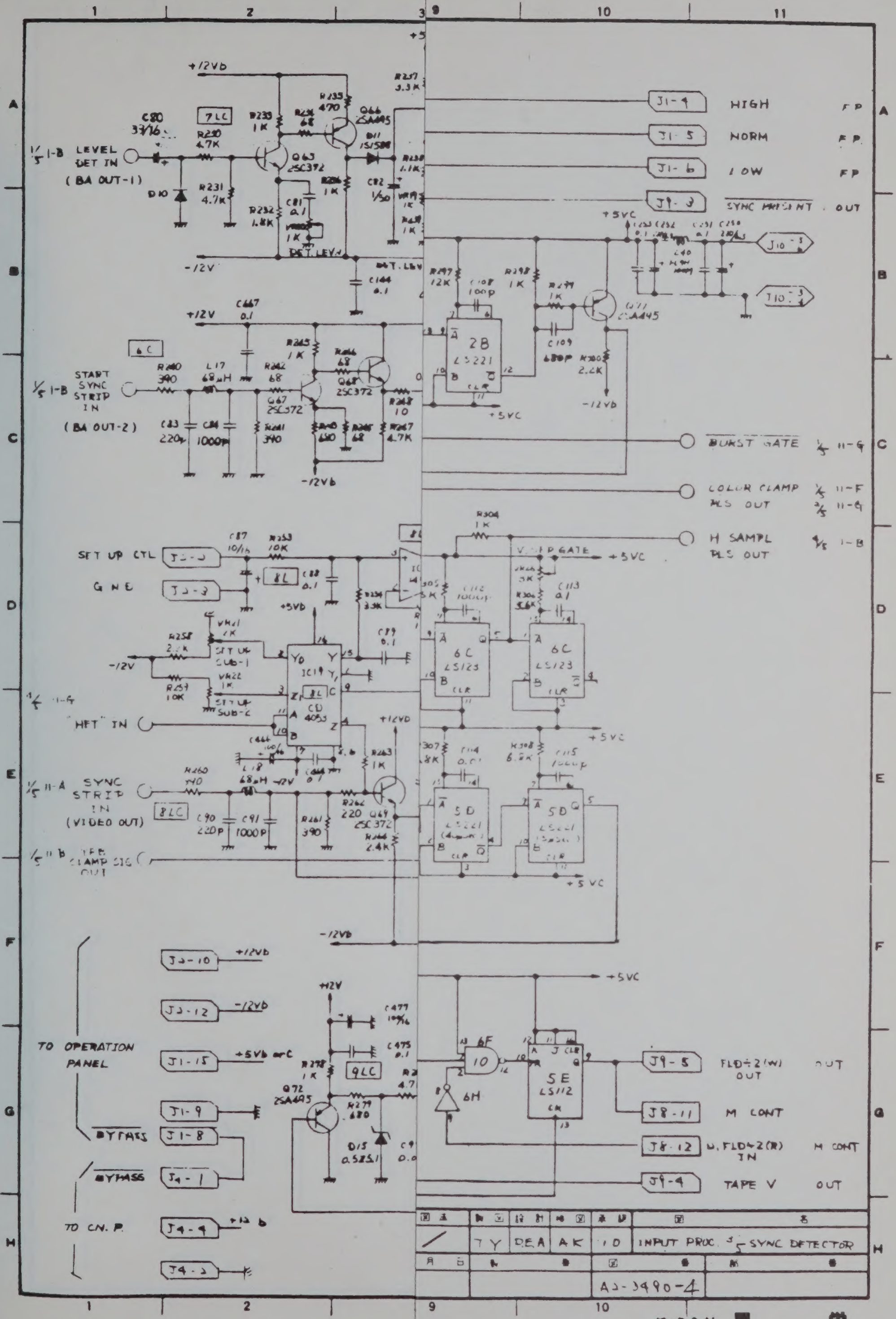
1
2
3
9
10
11
A
B
C
D
E
F
G
H
+12Vb
-12V
C80 33/16
7LC
R230 4.7K
R233 1K
R234 68
R235 470
Q66 2SA495
D11 1S1588
R237 3.3K
1/5 1-B LEVEL DET IN (BA OUT-1)
D10
R231 4.7K
Q63 2SC372
R232 1.8K
C81 0.1
R236 1K
C82 1/50
VR 1K
DET. LEV
C144 0.1
J1-4
HIGH
FP
J1-5
NORM
FP
J1-6
LOW
FP
J9-2
SYNC PRESENT
OUT
+5VC
J10
+12V
C467 0.1
6C
R245 1K
R246 68
Q68 2SC372
R240 390
L17 68μH
R242 68
1/5 1-B START SYNC STRIP IN (BA OUT-2)
Q67 2SC372
C83 220p
C84 1000p
R241 390
R248 10
R247 4.7K
-12Vb
R297 12K
C108 100p
2B
LS221
R298 1K
R299 1K
Q71 2SA495
C109 680P
R300 2.2K
-12Vb
BURST GATE
1/5 11-G
COLOR CLAMP PLS OUT
1/5 11-F
2/5 11-G
H SAMPL PLS OUT
4/5 1-B
R304 1K
C87 10/16
R253 10K
SET UP CTL
J2-2
GND
J2-3
8L
C88 0.1
R254 3.3K
V. SAMP GATE
+5VC
R305 3K
C112 1000p
R306 5.6K
C113 0.1
6C
LS123
+5VD
VR21 1K
R258 2.2K
SET UP SUB-1
IC19
CD 4053
VR22 1K
R257 10K
SET UP SUB-2
C79 0.1
4/5 11-G
"HFT" IN
+12VD
C466
L18 68μH
R260 390
1/5 11-A SYNC STRIP IN (VIDEO OUT)
8LC
C90 220P
C91 1000P
R261 390
R262 220
Q69 2SC372
R263 1K
R264 2.4K
R307 1.8K
C114 0.01
R308 6.8K
C115 1000p
5D
LS221
1/5 11b TEB CLAMP SIG OUT
-12Vb
J2-10
+12Vb
J2-12
-12Vb
TO OPERATION PANEL
J1-15
+5Vb or C
J1-9
BYPASS
J1-8
J4-1
TO CN. P.
J4-4
+12 b
J4-2
+12V
C477 10/16
C475 0.1
R278 1K
9LC
Q72 2SA495
R279 680
D15 05Z5.1
6F
10
6H
5E
LS112
J9-5
FLD÷2(W) OUT
OUT
J8-11
M CONT
J8-12
U. FLD÷2(R) IN
M CONT
J9-4
TAPE V
OUT
TY
DEA
AK
ID
INPUT PROC. & SYNC DETECTOR
AJ-3490-4

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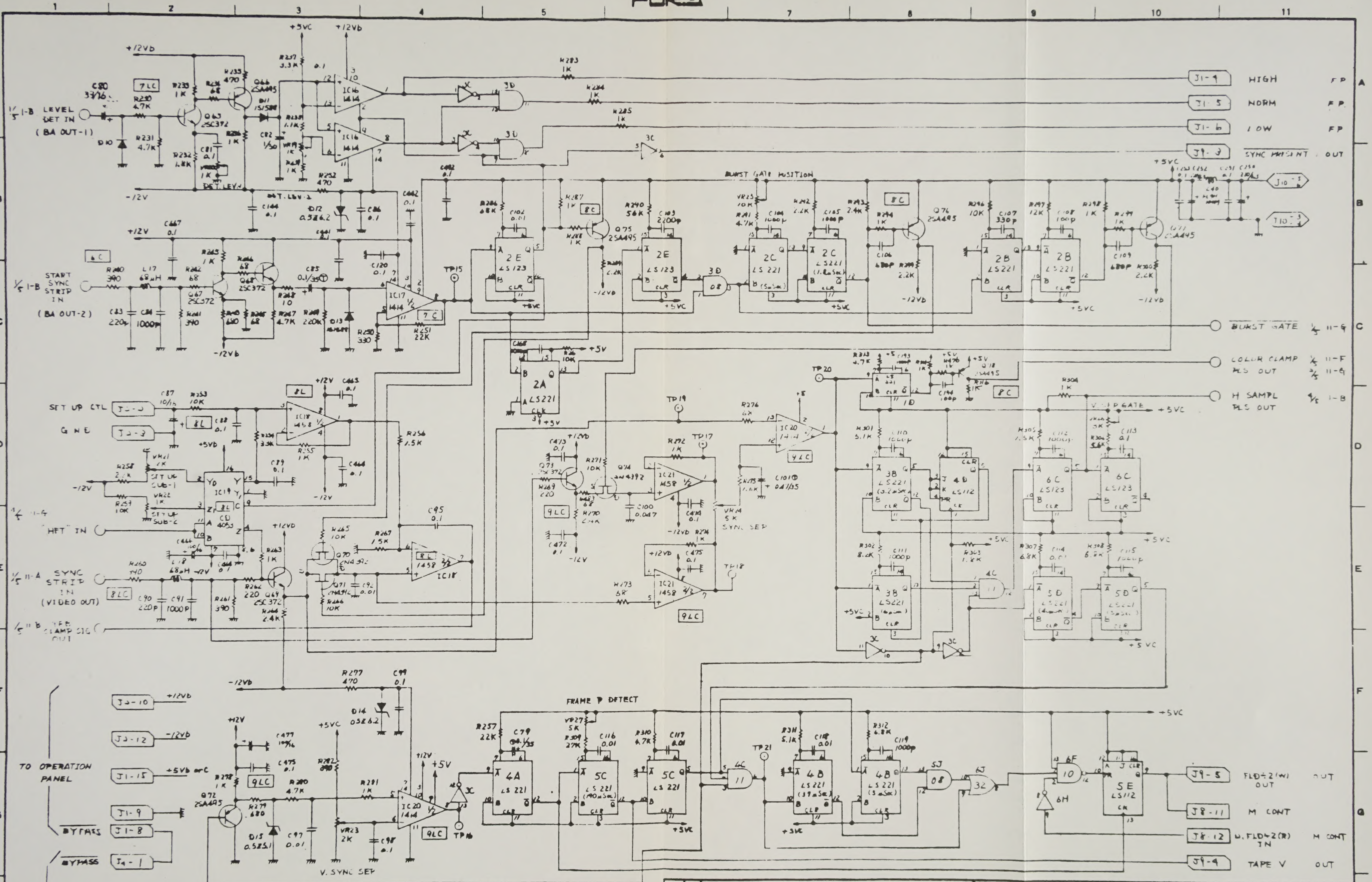
FOR-A


LEVEL DET IN (BA OUT-1)
START SYNC STRIP IN (BA OUT-2)
SET UP CTL
GND
"HET" IN
SYNC STRIP IN (VIDEO OUT)
REF CLAMP SIG OUT
TO OPERATION PANEL
TO CN. P.
BURST GATE POSITION
FRAME P DETECT
V. SYNC SEP
SYNC SEP
J1-4 HIGH F.P.
J1-5 NORM F.P.
J1-6 LOW F.P.
J9-3 SYNC PRESENT OUT
BURST GATE
COLOR CLAMP PLS OUT
H SAMPL PLS OUT
J9-5 FLD÷2(W) OUT
J8-11 M CONT
J8-12 W. FLD÷2(R) IN M CONT
J9-4 TAPE V OUT
J1-10 +12Vb
J1-12 -12Vb
J1-15 +5Vb or C
J1-9
J1-8 BYPASS
J4-1 BYPASS
J4-4 +12 b
J4-2
IC16 1414
IC17 1414
IC18 1458
IC19 CD4053
IC20 1414
IC21 MSP
IC21 1458
2E LS123
2C LS221
2B LS221
2A LS221
3B LS221
4D LS112
6C LS123
5D LS221
4A LS221
5C LS221
4B LS221
5E LS112
TP15
TP16
TP17
TP18
TP19
TP20
TP21

改訂	A

第三角図法	製図	設計	検図	承認	図名
尺度 /	TY	DEA	AK	10	INPUT PROC. & SYNC DETECTOR

作成 年 月 日	品番	図番	部番
枚数		A2-3490-4	

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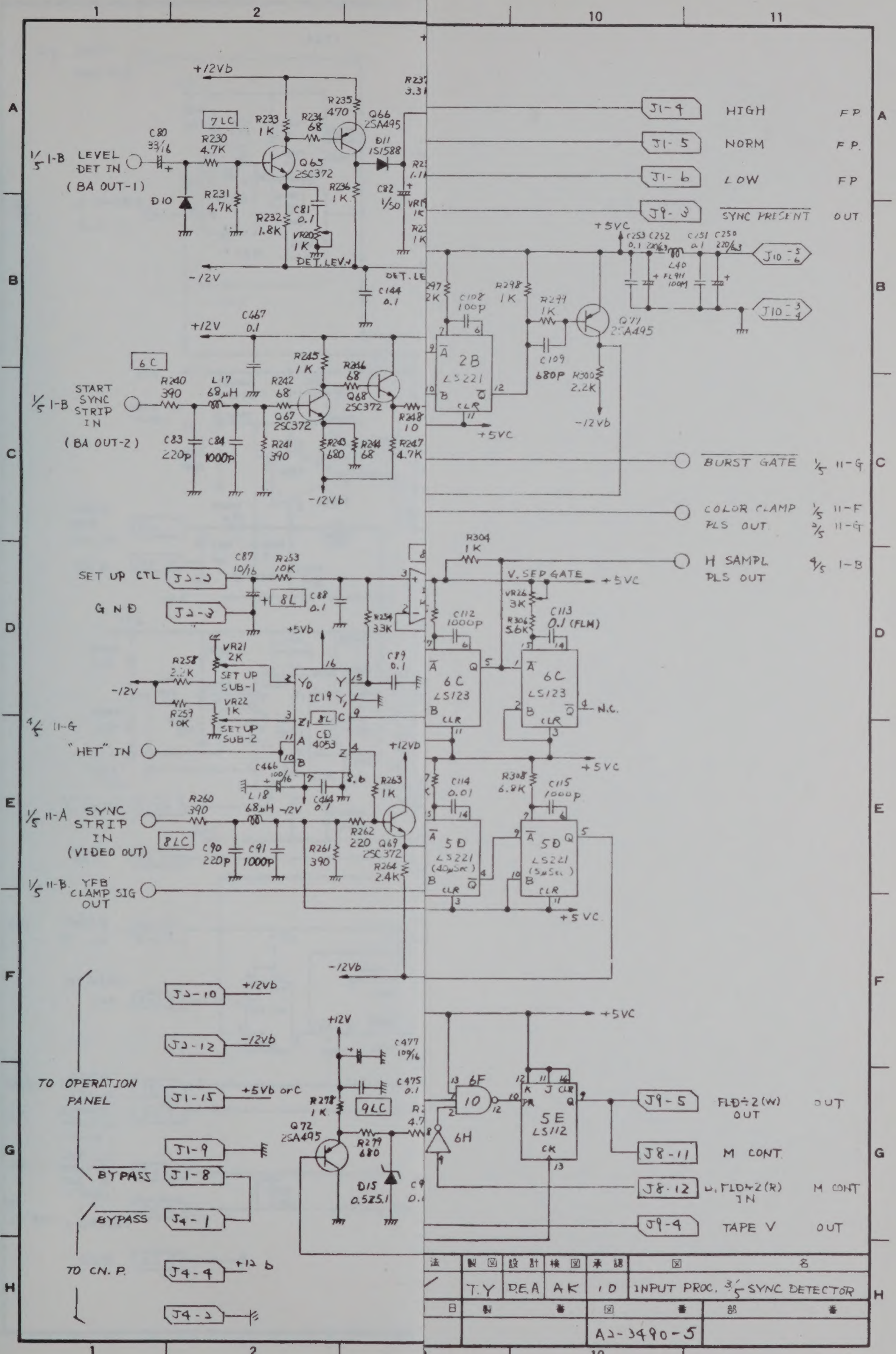

+12Vb
R237 3.3K
R235 470
Q66 2SA495
7LC
R233 1K
R234 68
D11 1S1588
C80 33/16
R230 4.7K
1/5 1-B LEVEL DET IN (BA OUT-1)
Q65 2SC372
D10
R231 4.7K
R236 1K
C82 1/50
R232 1.8K
C81 0.1
VR20 1K
DET. LEV.
-12V
C144 0.1
J1-4 HIGH FP
J1-5 NORM FP
J1-6 LOW FP
J9-3 SYNC PRESENT OUT
+5VC
C253 0.1
C252 220/6.3
C251 0.1
C250 220/6.3
L40 FL911 100M
J10-5/6
J10-3/4
R298 1K
R299 1K
C108 100P
Q77 2SA495
2B LS221
C109 680P
R300 2.2K
-12Vb
+12V
C467 0.1
6C
R245 1K
R246 68
Q68 2SC372
1/5 1-B START SYNC STRIP IN (BA OUT-2)
R240 390
L17 68μH
R242 68
Q67 2SC372
R248 10
C83 220P
C84 1000P
R241 390
R243 680
R244 68
R247 4.7K
BURST GATE 1/5 11-G
COLOR CLAMP PLS OUT 1/5 11-F 2/5 11-G
H SAMPL PLS OUT 4/5 1-B
R304 1K
SET UP CTL J2-2
C87 10/16
R253 10K
V. SEP GATE
GND J2-3
8L
C88 0.1
R254 33K
VR26 3K
C112 1000P
C113 0.1 (FLM)
R306 5.6K
+5Vb
VR21 2K
R258 2.2K
SET UP SUB-1
C89 0.1
6C LS123
N.C.
IC19 CD 4053
VR22 1K
R257 10K
SET UP SUB-2
4/5 11-G "HET" IN
C466 100/16
+12Vb
C114 0.01
R308 6.8K
C115 1000P
R263 1K
L18 68μH
C464 0.1
1/5 11-A SYNC STRIP IN (VIDEO OUT)
R260 390
8LC
C90 220P
C91 1000P
R262 220
Q69 2SC372
R261 390
R264 2.4K
5D LS221 (40μSec)
5D LS221 (5μSec)
1/5 11-B YFB CLAMP SIG OUT
J2-10 +12Vb
J2-12 -12Vb
TO OPERATION PANEL
J1-15 +5Vb or C
J1-9
BYPASS J1-8
BYPASS J4-1
TO CN. P.
J4-4 +12 b
J4-2
+12V
C477 10/16
C475 0.1
R278 1K
9LC
Q72 2SA495
R279 680
D15 0.5Z5.1
6F
6H
5E LS112
J9-5 FLD÷2 (W) OUT
J8-11 M CONT
J8-12 FLD÷2 (R) IN M CONT
J9-4 TAPE V OUT

法	製図	設計	検図	承認	図名
	T.Y	DEA	AK	ID	INPUT PROC. 3/5 SYNC DETECTOR

日	製番	図番	部番
		A2-3490-5	

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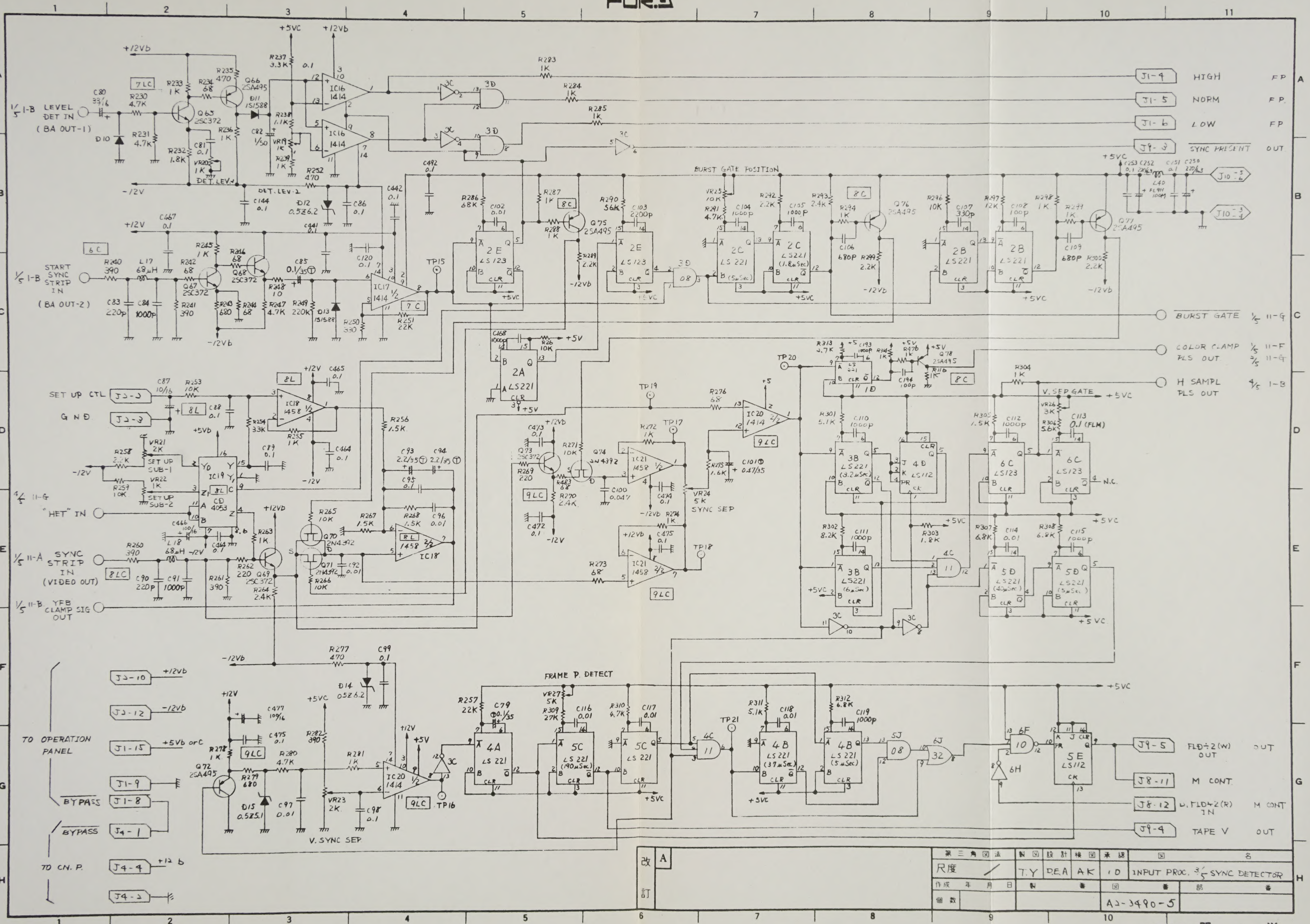
FOR.A


1/5 1-B LEVEL DET IN (BA OUT-1)
1/5 1-B START SYNC STRIP IN (BA OUT-2)
SET UP CTL J2-2
GND J2-3
4/5 11-G "HET" IN
1/5 11-A SYNC STRIP IN (VIDEO OUT)
1/5 11-B YFB CLAMP SIG OUT
DET. LEV-1
DET. LEV-2
BURST GATE POSITION
J1-4 HIGH FP
J1-5 NORM FP
J1-6 LOW FP
J9-3 SYNC PRESENT OUT
J10-5/6
J10-3/4
BURST GATE 1/5 11-G
COLOR CLAMP PLS OUT 1/5 11-F 2/5 11-G
H SAMPL PLS OUT 4/5 1-B
V. SEP GATE
SYNC SEP
V. SYNC SEP
FRAME P. DETECT
TO OPERATION PANEL
J2-10 +12Vb
J2-12 -12Vb
J1-15 +5Vb or C
J1-9
BYPASS J1-8
BYPASS J4-1
TO CN. P.
J4-4 +12 b
J4-2
J9-5 FLD÷2(W) OUT
J8-11 M CONT
J8-12 D. FLD÷2(R) IN M CONT
J9-4 TAPE V OUT
IC16 1414
IC17 1414
IC18 1458
IC19 CD 4053
IC20 1414
IC21 1458
2E LS123
2C LS221 (5μSec)
2C LS221 (1.8μSec)
2B LS221
2A LS221
1D LS221
3B LS221 (3.2μSec)
3B LS221 (6μSec)
4D LS112
6C LS123
5D LS221 (40μSec)
5D LS221 (5μSec)
4A LS221
5C LS221 (190μSec)
5C LS221
4B LS221 (37μSec)
4B LS221 (5μSec)
5E LS112
Q63 2SC372
Q66 2SA495
Q67 2SC372
Q68 2SC372
Q69 2SC372
Q70 2N4392
Q71 2N4392
Q72 2SA495
Q73 2SC372
Q74 2N4392
Q75 2SA495
Q76 2SA495
Q77 2SA495
Q78 2SA495
TP15
TP16
TP17
TP18
TP19
TP20
TP21
+5VC
+12Vb
-12Vb
+12V
-12V
+5V
1
2
3
4
5
6
7
8
9
10
11
A
B
C
D
E
F
G
H

改 訂	A	第三角図法	製図	設計	検図	承認	図名	
		尺度 /	T.Y	DEA	AK	ID	INPUT PROC. 3/5 SYNC DETECTOR	
		作成 年 月 日	製番			図番		部番
		個数				A2-3490-5		

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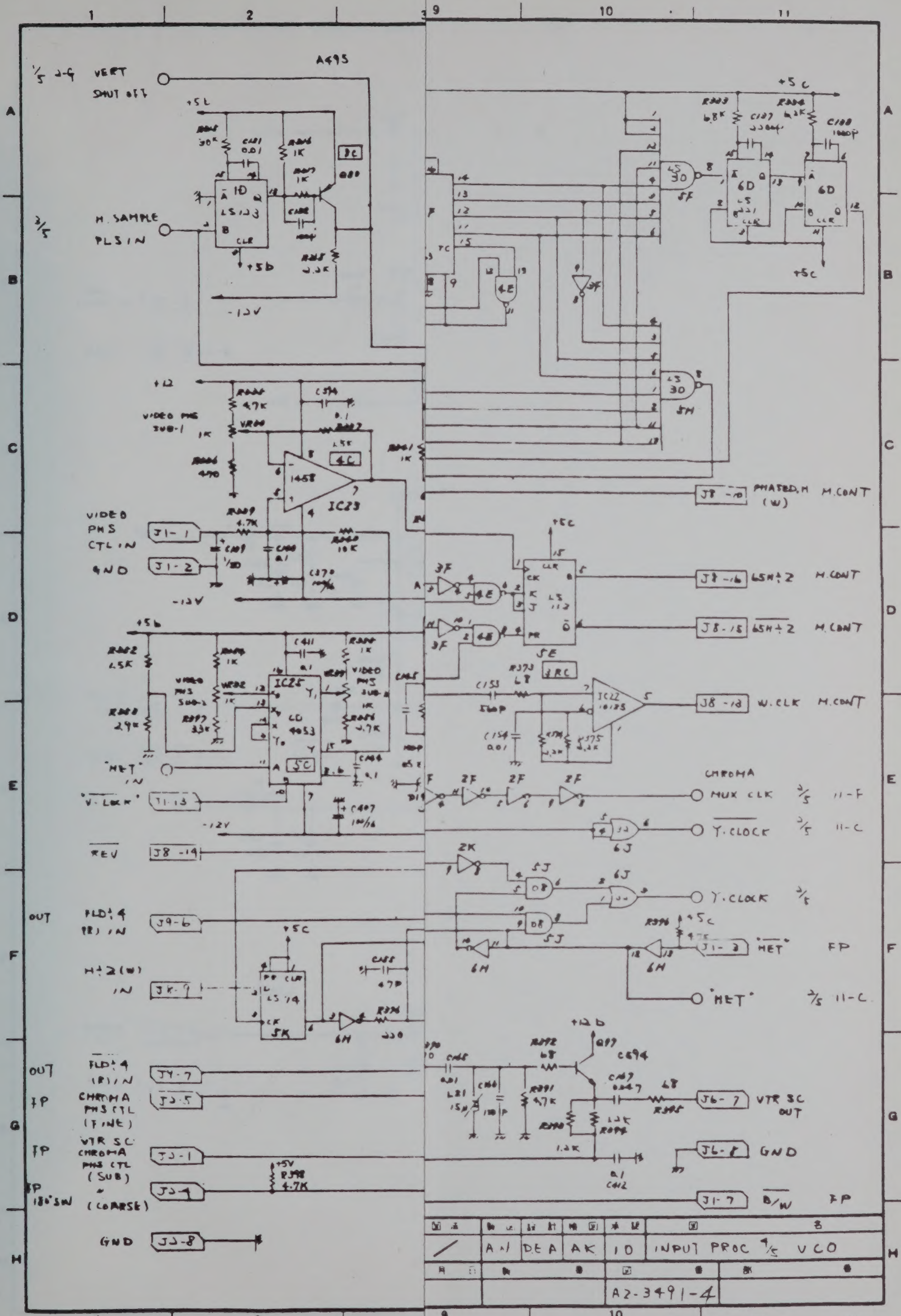
1
2
3
9
10
11
A
B
C
D
E
F
G
H
A495
1/5 2-G VERT SHUT OFF
+5L
30K
0.01
1K
1D
LS123
Q80
3/5 H. SAMPLE PLS IN
+5b
2.2K
-12V
+5C
6.8K
1K
1000P
LS30
5F
6D
LS221
3F
4E
LS30
5H
+12
4.7K
VIDEO PHS SUB-1
1K
470
0.1
1.5K
4C
1458
IC23
J8-10 PHASED.H (W) M.CONT
VIDEO PHS CTL IN
J1-1
4.7K
10K
GND
J1-2
-12V
+5C
3F
4E
LS112
5E
J8-16 65H÷2 M.CONT
J8-15 65H÷2 M.CONT
+5b
1.5K
1K
IC25
CD4053
5C
VIDEO PHS SUB-2
33K
2.7K
24K
R373
68
3RC
C153 560P
IC22 10125
C154 0.01
J8-18 W.CLK M.CONT
"HET" IN
"V-LOCK" J1-13
3F
2F
2F
2F
CHROMA MUX CLK 3/5 11-F
Y.CLOCK 3/5 11-C
6J
-12V
100/16
REV J8-19
2K
5J
6J
Y.CLOCK 3/5
OUT FLD÷4 (R) IN J9-6
5J
6H
+5C
HET FP J1-3
6H
+5C
"HET" 3/5 11-C
H÷2(W) IN JK-9
LS74
5K
47P
6H
220
+12b
Q97
C694
68
OUT FLD÷4 (R) IN J4-7
FP CHROMA PHS CTL (FINE) J2-5
0.01
15μ
4.7K
0.047
68
J6-7 VTR SC OUT
1.2K
1.2K
FP VTR SC CHROMA PHS CTL (SUB) J2-1
J6-8 GND
0.1
+5V R398 4.7K
FP 180°SW (COARSE) J2-4
J1-7 B/W FP
GND J2-8

A-1	DEA	AK	10	INPUT PROC 4/5 VCO

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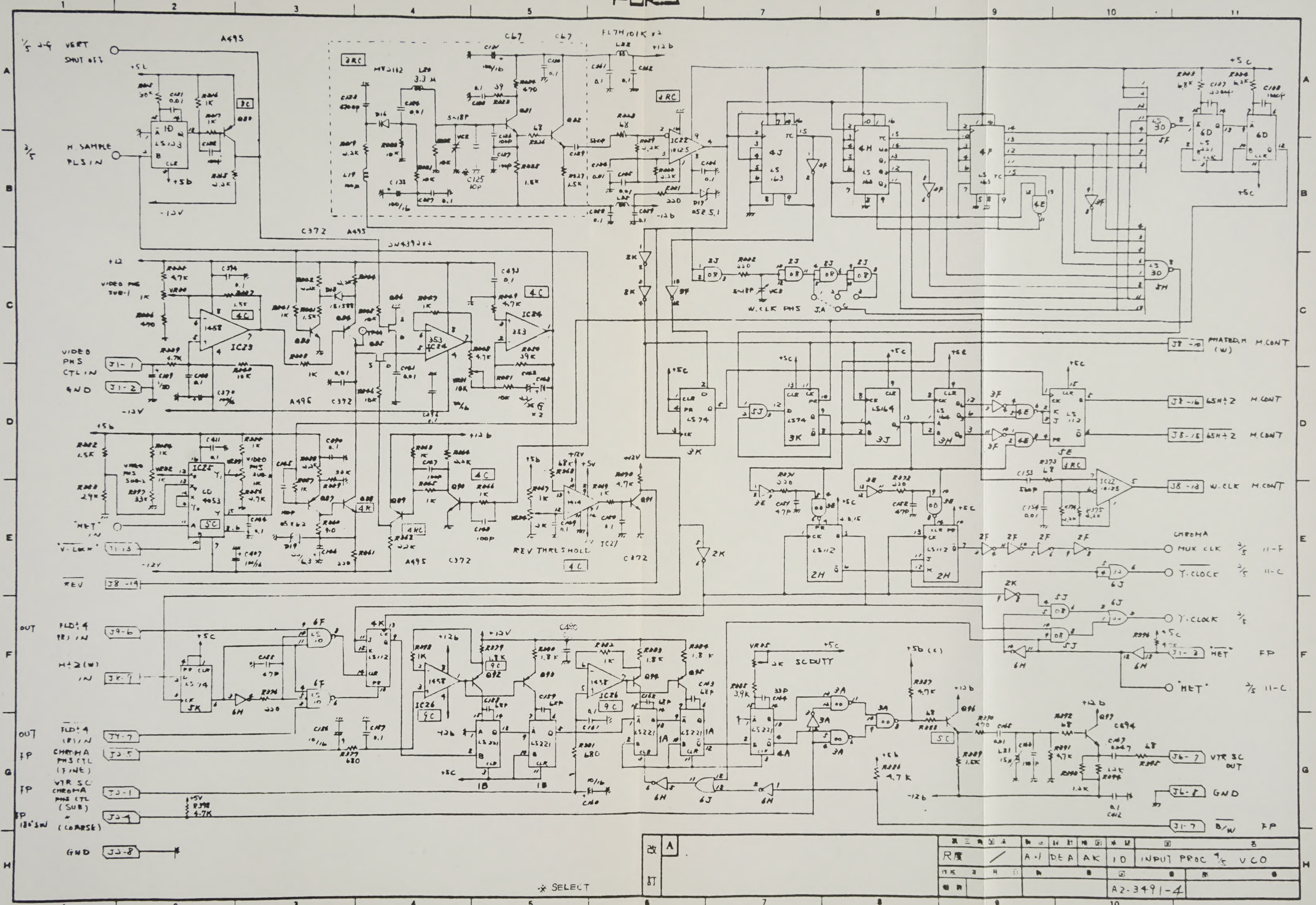
FOR-A


1/5 2-G VERT SHUT OFF
H. SAMPLE PLS IN
2/5
LS123
-12V
3RC
MV2102
3.3 M
SN18P
C125 10P
FL7H101K ×2
+12b
IC22 10125
4J LS163
4H LS163
4F LS163
3E
LS30 5F
6D LS221
+5c
LS30 5H
2J
W. CLK PHS
JA
SN439202
VIDEO PHS SUB-1
1458 IC23
353 IC24
IC24 353
VIDEO PHS CTL IN
GND
J1-1
J1-2
A495
C372
4C
"HET" IN
"V-LOCK" J1-13
4053 IC25 5C
VIDEO PHS SUB-2
VIDEO PHS SUB-1
4K
4KC
REV THRESHOLD
1414 IC27
REV J8-14
LS74 3K
LS74 3K
LS164 3J
LS164 3H
LS112 5E
J8-10 PHASED.H (W) H.CONT
J8-16 65H÷2 H.CONT
J8-15 65H÷2 H.CONT
J8-18 W.CLK H.CONT
IC22 10125
LS112 2H
CHROMA MUX CLK 3/5 11-F
Y. CLOCK 3/5 11-C
Y. CLOCK 3/5
"HET" FP
"HET" 3/5 11-C
OUT FLD÷4 (B) IN J9-6
H÷2(W) IN J8-9
LS74 5K
6F
4K LS112
1458 IC26
LS221 1B
9C
C490
SC DUTY
LS221 1A
LS221 4A
3A
5C
OUT FLD÷4 (R) IN J9-7
FP CHROMA PHS CTL (FINE) J3-5
FP VTR SC CHROMA PHS CTL (SUB) J3-1
FP 180°SW (COARSE) J3-9
GND J3-8
R398 4.7K
6H
6J
J6-7 VTR SC OUT
J6-8 GND
J1-7 B/W FP
※ SELECT

第三角図法	製図	設計	検図	承認	図名
尺度 /	A-1	DE A	AK	10	INPUT PROC 4/5 VCO
作成 年 月 日	納入先		図番 A2-3491-4	部番	
備考					

改訂 A

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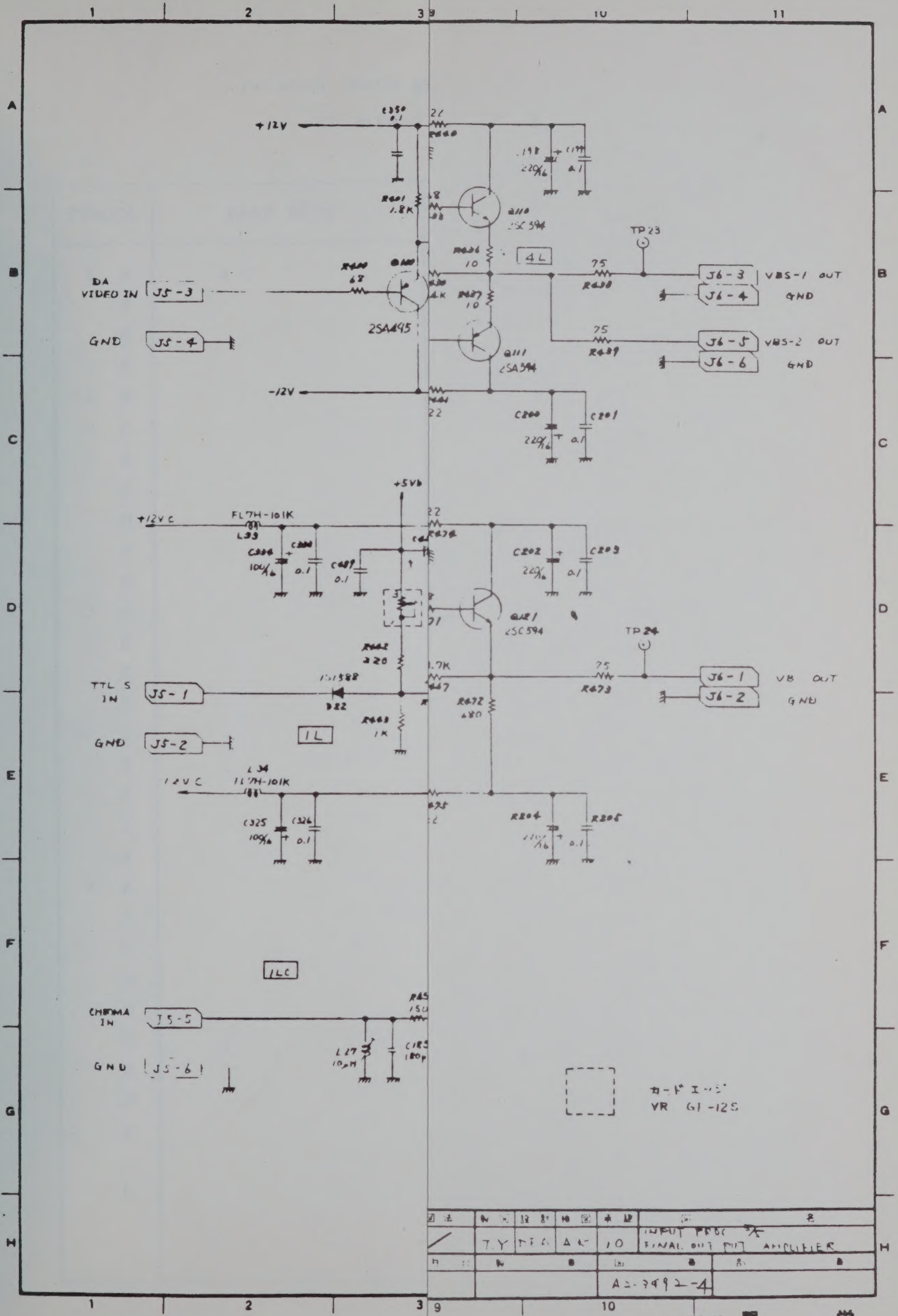+12V
C350
0.1
22
R400
R401
1.8K
Q110
2SC594
R406
10
4L
DA
VIDEO IN
J5-3
68
Q100
2SA495
R407
10
Q111
2SA594
GND
J5-4
-12V
22
220/16
C200
C201
0.1
TP23
75
R438
J6-3
VBS-1 OUT
J6-4
GND
75
R439
J6-5
VBS-2 OUT
J6-6
GND
+5Vb
+12VC
FL7H-101K
L33
C204
100/16
0.1
C489
0.1
22
C202
220/16
C203
0.1
Q121
2SC594
R462
220
1.7K
1S1588
D22
TTL S
IN
J5-1
GND
J5-2
1L
R463
1K
R472
680
TP24
75
R473
J6-1
VB OUT
J6-2
GND
L34
FL7H-101K
12VC
C325
100/16
C326
0.1
22
R204
R205
0.1
1LC
CHROMA
IN
J5-5
GND
J5-6
L27
10μH
150
180p
カードエッジ
VR GI-12S
T.Y
10
INPUT PROC 5/5
FINAL OUT PUT AMPLIFIER
A2-3492-4
A
B
C
D
E
F
G
H
1
2
3
9
10
11

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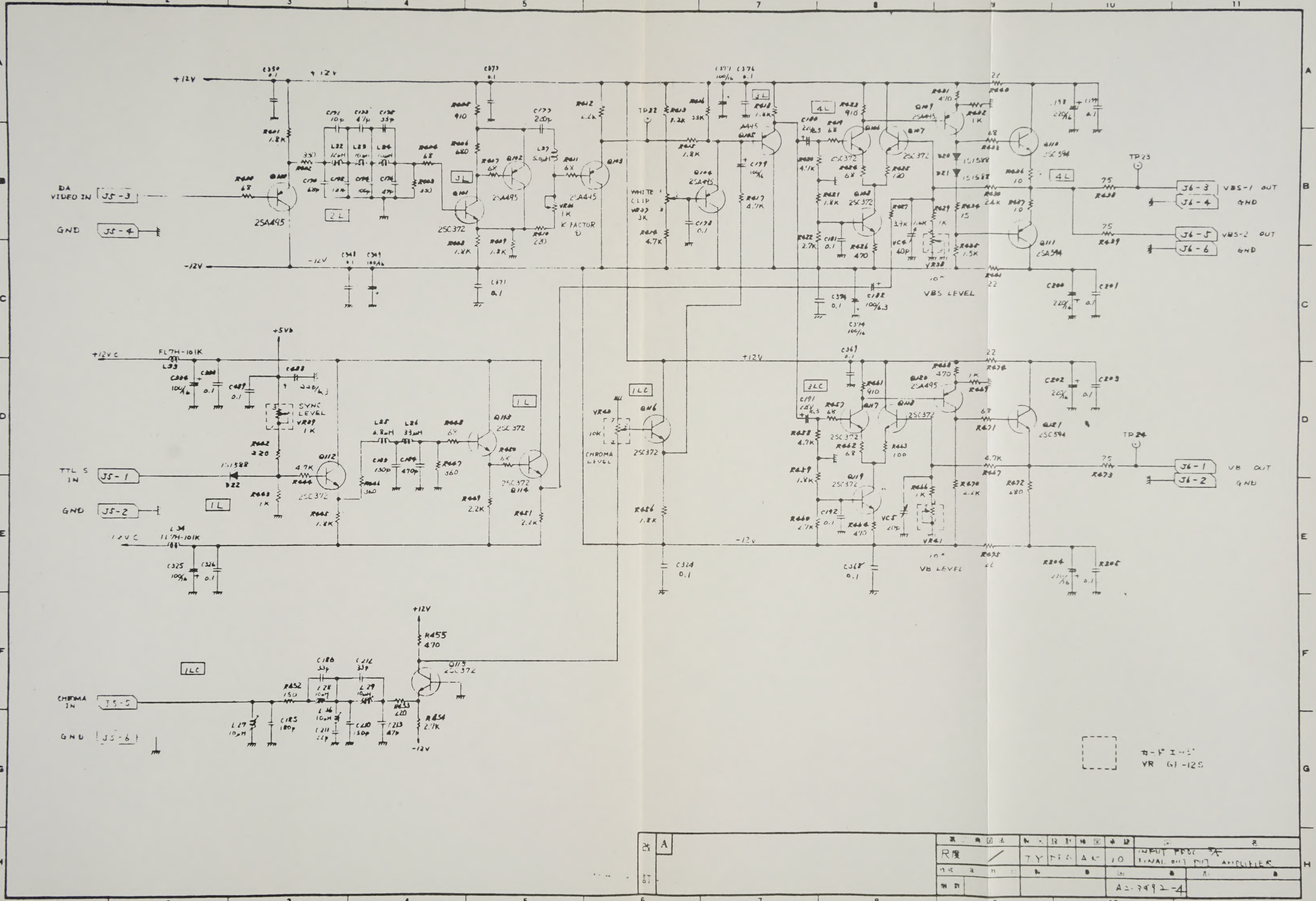
+12V
-12V
DA VIDEO IN
J5-3
GND
J5-4
2SA495
2SC372
2SA445
2SC594
K FACTOR
WHITE CLIP
TP22
TP23
TP24
VBS LEVEL
VB LEVEL
J6-3
VBS-1 OUT
J6-4
GND
J6-5
VBS-2 OUT
J6-6
J6-1
VB OUT
J6-2
+5VD
+12VC
-12VC
FL7H-101K
SYNC LEVEL
VR89
TTL S IN
J5-1
J5-2
1S1588
CHROMA LEVEL
CHROMA IN
J5-5
J5-6
R455
470
Q115
2SC372
R454
2.7K
1L
2L
3L
4L
1LC
3LC
カード エッジ
VR GI-12S

尺度
T.Y
10
INPUT PROC 基
FINAL OUT PUT AMPLIFIER
A2-3492-4

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FA-410N INPUT PROCESSOR BOARD

A2~3488-2~3492-2

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
1 A	I C	SN 74 LS 221	
B		"	
D		123	
E		08	
2 B		221	
C		"	
E		123	
F		04	
H		112	
J		08	
K		04	
3 A		00	
B		221	
C		04	
D		08	
E		00	
F		04	
H		164	
J		"	
K		74	
4 A		221	
B		"	
C		11	
D		112	
E		00	
F		163	
H		"	
J		"	
K		112	
C		221	
D		"	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
5 E	I C	SN 74 LS 112	
F		30	
H		"	
J		08	
K		74	
C		123	
D		221	
F		10	
H		04	
J		32	
K		00	
A		221	
IC 1	I C	MC 1495	with IC socket
2		DG 301 CJ	
3		MC 1458	
4		CD 4051	
5		LM 1848 N	
6		LM 308	
7		Deleted	
8		LM 361 J	
9		TCD 1007	
10		"	
11		SN 74 LS 374	
12		"	
13		HD 10124	
14		CD 4053 BE	
15		MC 1458	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
IC 16	I C	MC 1414	
17		"	
18		MC 1458	
19		CD 4053 BE	
20		MC 1414	
21		MC 1458	
22		HD 10125	
23		MC 1458	
24		LF 353	
25		CD 4053	
26		MC 1458	
27		MC 1414	
28		SN 74LS 123	
Q 1	Transistor	2 SC 372	
2		2 SA 495	
3		2 SC 372	
4		"	
5		"	
6		2 SA 495	
7		2 SC 372	
8		"	
9		"	
10		"	
11		"	
12		"	
13		2 SA 495	
14		2 SC 372	
15		2 SA 495	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
Q 16	Transistor	2 SC 372	
17		2 SA 495	
18		2 SC 372	
19		2 SA 495	
20		2 SC 372	
21		2 SA 495	
22		2 SC 372	
23		"	
24		2 SA 495	
25		2 SC 372	
26		"	
27		"	
28		"	
29		"	
30		"	
31		"	
32		"	
33		"	
34		"	
35		"	
36		2 N 4392	
37		2 SC 372	
38		"	
39		2 SA 495	
40		2 N 4392	
41		2 SC 372	
42		"	
43		Deleted	
44		2 SA 495	
45		2 SA "	

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
Q 46	Transistor	2 SC 372	
47		"	
48		2 SA 495	
49		2 SC 372	
50		"	
51		2 SC 67	
52		"	
53		2 SC 372	
54		2 SC 67	
55		"	
56		2 SC 372	
57		"	
58		"	
59		"	
60		"	
61		"	
62		Deleted	
63		"	
64		"	
65		2 SC 372	
66		Deleted	
67		2 SC 372	
68		"	
69		"	
70		2 N 4392	
71		"	
72		2 SA 495	
73		2 SC 372	
74		2 N 4392	
75		2 SA 495	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
Q 76	Transistor	2 SA 495	
77		"	
78		"	
79		Deleted	
80		2 SA 495	
81		2 SC 67	
82		"	
83		2 SC 372	
84		2 SA 495	
85		2 N 4392	
86		"	
87		2 SA 495	
88		2 SC 372	
89		2 SA 495	
90		2 SC 372	
91		"	
92		2 SA 495	
93		"	
94		"	
95		"	
96		2 SC 372	
97		2 SC 594	
98		Deleted	
99		Deleted	
100		2 SA 495	
101		2 SC 372	
102		2 SA 495	
103		"	
104		"	
105		"	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
Q 106	Transistor	2 SC 372	
107		"	
108		"	
109		2 SA 495	
110		2 SC 594	
111		2 SA 594	
112		2 SC 372	
113		"	
114		"	
115		"	
116		"	
117		"	
118		"	
119		"	
120		2 SA 495	
121		2 SC 594	
PC 1	Photocoupler	VTL 5C 412	
D 1	Diode	IS 1588	
2		05Z 5.1	
3		MV 2108	
4		Deleted	
5		MC 911	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
D 6	Diode	MC 921	
7		MC 911	
8		MC 921	
9		05Z 5.1	
10		Deleted	
11		IS 1588	
12		05Z 6.2	
13		IS 1588	
14		05Z 6.2	
15		05Z 5.1	
16		MV 2112	
17		05Z 5.1	
18		IS 1588	
19		05Z 6.2	
20		IS 1588	
21		"	
22		"	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
R 1	Fixed Resistor	CR 25J 750	
2		472	
3		680	
4		472	
5		102	
6		681	
7		911	
8		182	
9		221	
10		152	
11		680	
12		681	
13		470	
14		102	
15		562	
16		102	
17		102	
18		622	
19		"	
20		681	
21		271	
22		103	
23		223	
24		182	
25		182	
26		103	
27		680	
28		122	
29		301	
30		392	

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
R 31	Fixed Resistor	CR 25JU 301	
32		680	
33		162	
34		821	
35		122	
36		680	
37		472	
38		182	
39		102	
40		332	
41		562	
42		182	
43		911	
44		182	
45		102	
46		"	
47		680	
48		561	
49		182	
50		680	
51		472	
52		680	
53		242	
54		683	
55		"	
56		"	
57		222	
58		471	
59		104	
60		332	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
R 61	Fixed Resistor	CR 25JU 472	
62		752	
63		104	
64		473	
65		104	
66		103	
67		680	
68		681	
69		911	
70		182	
71		221	
72		152	
73		680	
74		681	
75		911	
76		182	
77		221	
78		242	
79		680	
80		472	
81		680	
82		332	
83		562	
84		182	
85		"	
86		"	
87		"	
88		102	
89		680	
90		561	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
R 91	Fixed Resistor	CR 25JU 182	
92		680	
93		681	
94		301	
95		471	
96		102	
97		301	
98		472	
99		301	
100		472	
101		"	
102		"	
103		152	
104		680	
105		472	
106		121	
107		242	
108		472	
109		Deleted	
110		102	
111		223	
112		242	
113		680	
114		242	
115		102	
116		"	
117		680	
118		471	
119		391	
120		102	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS		REMARKS
R 121	Fixed Resistor	CR 25JU	221	
122			471	
123			680	
124			242	
125			680	
126			242	
127			331	
128			471	
129			472	
130			680	
131			242	
132			680	
133			242	
134			223	
135			222	
136			473	
137			222	
138			473	
139			102	
140			334	
141			331	
142			473	
143			302	
144			472	
145			473	
146			152	
147			221	
148			242	
149			102	
150			242	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
R 151	Fixed Resistor	CR 25JU 103	
152		"	
153		102	
154		392	
155		103	
156		102	
157		301	
158		102	
159		Deleted	
160		680	
161		182	
162		680	
163		101	
164		102	
165		391	
166		6R8	
167		471	
168		681	
169		680	
170		182	
171		680	
172		101	
173		102	
174		391	
175		6R8	
176		222	
177		101	
178		222	
179		101	
180		472	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
R 181	Fixed Resistor	CR 25JU 331	
182		561	
183		681	
184		121	
185		680	
186		131	
187		472	
188		391	
189		102	
190		680	
191		182	
192		680	
193		182	
194		102	
195		561	
196		"	
197		102	
198		561	
199		"	
200		470	
201		"	
202		"	
203		182	
204		101	
205		122	
206		680	
207		153	
208		472	
209		121	
210		222	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
R 211	Fixed Resistor	CR 25JU 330	
212		153	
213		102	
214		680	
215		472	
216		"	
217		680	
218		122	
219		153	
220		472	
221		"	
222		"	
223		102	
224		223	
225		203	
226		680	
227		Deleted	
228		"	
229		"	
230		202	
231		332	
232		182	
233		102	
234		103	
235		391	
236		202	
237		332	
238		751	
239		102	
240		391	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
R 241	Fixed Resistor	CR 25JU 391	
242		680	
243		681	
244		680	
245		102	
246		680	
247		472	
248		100	
249		224	
250		331	
251		223	
252		471	
253		103	
254		333	
255		102	
256		152	
257		223	
258		222	
259		103	
260		391	
261		"	
262		221	
263		102	
264		242	
265		103	
266		"	
267		152	
268		Deleted	
269		221	
270		242	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
R 271	Fixed Resistor	CR 25JU 103	
272		102	
273		680	
274		102	
275		162	
276		680	
277		471	
278		102	
279		681	
280		472	
281		102	
282		391	
283		102	
284		"	
285		"	
286		683	
287		102	
288		"	
289		222	
290		563	
291		472	
292		222	
293		242	
294		102	
295		222	
296		103	
297		123	
298		102	
299		"	
300		222	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
R 301	Fixed Resistor	CR 25J 512	
302		822	
303		182	
304		102	
305		152	
306		562	
307		682	
308		"	
309		273	
310		472	
311		512	
312		682	
313		272	
314		102	
315		303	
316		102	
317		"	
318		222	
319		"	
320		103	
321		"	
322		"	
323		390	
324		471	
325		152	
326		680	
327		152	
328		680	
329		222	
330		"	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
R 331	Fixed Resistor	CR 25JU 221	
332		"	
333		682	
334		622	
335		472	
336		471	
337		152	
338		102	
339		472	
340		103	
341		102	
342		222	
343		152	
344		222	
345		103	
346		"	
347		102	
348		472	
349		"	
350		393	
351		103	
352		152	
353		392	
354		102	
355		"	
356		272	
357		102	
358		222	
359		332	
360		911	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS		REMARKS
R 361	Fixed Resistor	CR 25JU	221	
362			222	
363			102	
364			222	
365			102	
366			"	
367			"	
368			683	
369			102	
370			472	
371			221	
372			"	
373			680	
374			222	
375			"	
376			221	
378			681	
379			102	
380			182	
381			"	
382			681	
383			102	
384			182	
385			392	
386			472	
387			"	
388			"	
389			680	
390			152	
			471	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS		REMARKS
R 391	Fixed Resistor	CR 25JU	472	
392			680	
393			122	
394			"	
395			680	
396			472	
397			332	
398			472	
399		Deleted		
400			680	
401			182	
402			331	
403			"	
404			680	
405			911	
406			681	
407			680	
408			182	
409			"	
410			221	
411			680	
412			222	
413			122	
414			472	
415			182	
416			333	
417			472	
418			182	
419			680	
420			472	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
R 421	Fixed Resistor	CR 25JU 182	
422		272	
423		911	
424		680	
425		121	
426		471	
427		392	
428		Deleted	
429		102	
430		242	
431		471	
432		102	
433		680	
434		150	
435		152	
436		100	
437		"	
438		750	
439		"	
440		220	
441		"	
442		221	
443		102	
444		472	
445		182	
446		361	
447		"	
448		680	
459		222	
460		680	

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
R 451	Fixed Resistor	CR 25JU 222	
452		151	
453		221	
454		272	
455		471	
456		182	
457		680	
458		472	
459		182	
460		272	
461		911	
462		680	
463		101	
464		471	
465		Deleted	
466		102	
467		472	
468		471	
469		102	
470		222	
471		680	
472		681	
473		750	
474		220	
475		"	
476		102	
477		Deleted	
478		Deleted	
479		Deleted	
480		223	

FA-410N INPUT PTOCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
R 481	Fixed Resistor	CR 25JU 221	
482		472	
483		680	
486		102	
487		104	
484		473	
RA 1	Resistor Array	EXB-P8 8 222	
2		"	
VR 1	Variable Resistor	GFP 06 102	
2		502	
3		103	
4		"	
5		102	
6		"	
7		102	
8		501	
9		102	
10		201	
11		"	
12		101	
13		102	
14		202	
15		102	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS		REMARKS
VR 16	Variable Resistor	GEP 06	102	
17			"	
18			202	
19		Deleted		
20			102	
21			202	
22			102	
23			202	
24			502	
25			103	
26			302	
27			502	
28		Deleted		
29		Deleted		
30			102	
31			103	
32			102	
33			"	
34			202	
35			"	
36			102	
37			302	
38		GF-12S	103	
39			102	
40			103	
41			"	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 1	Electrolytic	6.3R 221	
2	Dip Mica	DM 101 J	
3	Electrolytic	6.3R 471	
4	Dip Mica	DM 470 J	
5	Stacking Ceramic	RPE 122C 104Z 50	
6	Electrolytic	16R 221	
7	Stacking Ceramic	RPE 122C 104Z 50	
8	Electrolytic	16R 221	
9	Dip Mica	DM 121 J	
10		221J	
11		"	
12		510 J	
13	Electrolytic	16R 221	
14	Stacking Ceramic	RPE 122C 104Z 50	
15		"	
16		"	
17	Dip Mica	DM 181 J	
18		361 J	
19	Electrolytic	16R 221	
20	Dip Mica	DM 201 J	
21		330 J	
22		271 J	
23		221 J	
24		391 J	
25		121 J	
26		151 J	
27	Electrolytic	6.3R 471	
28	Stacking Ceramic	RPE 1220 104Z 50	
29	Dip Mica	DM 101J	
30	Stacking Ceramic	16R 221	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 31	Film	CQ 92 1H 103	
32	Dip Mica	DM 151J	
33	Film	CQ 92 1H 102	
34	Dip Mica	DM 151J	
35	Film	CQ 92 1H 103	
36		"	
37	Electrolytic	16R 221	
38	Dip Mica	DM 511J	
39		180J	
40		511J	
41	Tantal	1μF 35V	
42	Dip Mica	DM 511J	
43		180J	
44		511J	
45	Tantal	1μF 35V	
46	Film	CQ 92 1H 103	
47	Stacking Ceramic	RPE 122C 104Z 50	
48	Film	CQ 92 1H 103	
49	Electrolytic	16R 100	
50	Stacking Ceramic	RPE 122C 104Z 50	
51	Film	CQ 92 1H 103	
52	Dip Mica	DM 391J	
53		620J	
54	Film	CQ 92 1H 103	
55		"	
56	Dip Mica	DM 221J	
57	Film	CQ 92 1H 103	
58	Dip Mica	DM 101J	
59	Electrolytic	16R 221	
60	Stacking Ceramic	RPE 122C 104Z 50	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 61	Electrolytic	6.3R 101	
62	Dip Mica	DM 390J	
63	Stacking Ceramic	RPE 122C 104Z 50	
64	Electrolytic	6.3R 101	
65	Film	CQ 92 1H 223	
66	Stacking Ceramic	RPE 122C 104Z 50	
67	Film	CQ 92 1H 223	
68	Stacking Ceramic	RPE 122C 104Z 50	
69		"	
70	Electrolytic	6.3R 101 N.P.	
71		16R 101	
72	Tantal	1μF 35V	
73	Dip Mica	DM 390J	
74	Electrolytic	6.3R 101	
75	Stacking Ceramic	RPE 122C 104Z 50	
76	Electrolytic	6.3R 101	
77	Stacking Ceramic	RPE 122C 104Z 50	
78	Dip Mica	DM 100J	
79	Tantal	0.1μF 35V	
80	Electrolytic	ECEAICS 330	
81	Stacking Ceramic	RPE 122C 104Z 50	
82	Electrolytic	50R 1R0	
83	Dip Mica	DM 221J	
84	Film	CQD 921H 0.001U	
85	Tantal	0.1μF 35V	
86	Stacking Ceramic	RPE 122C 104Z 50	
87	Electrolytic	16R 100	
88	Stacking Ceramic	RPE 122C 104Z 50	
89		"	
90	Dip Mica	DM 221J	

FA-410N INPUR PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 91	Film	CQD 921H 0.001U	
92	Film	CQ 92 1H 103	
93		Deleted	
94		"	
95	Stacking Ceramic	RPE 122C 104Z 50	
96		Deleted	
97	Film	CQ 92 1H 103	
98	Stacking Ceramic	RPE 122C 104Z 50	
99		"	
100	Film	CQ 92 1H 473	
101	Tantal	0.47μF 35V	
102	Film	CQ 92 1H 103	
103		222	
104		102	
105		"	
106	Dip Mica	DM 681J	
107		331J	
108		101J	
109		681J	
110	Film	CQ 92 1H 102	
111		"	
112		"	
113		104	
114		103	
115		102	
116		103	
117		"	
118		"	
119		102	
120	Stacking Ceramic	RPE 122C 104Z 50	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 121	Film	CQ 92 1H 103	
122	Dip Mica	DM 101J	
123	Film	CQ 92 1H 472	
124		103	
125		Select	
126	Dip Mica	101J	
127		"	
128	Stacking Ceramic	RPE 122C 104Z 50	
129	Dip Mica	DM 561J	
130	Stacking Ceramic	RPE 122C 104Z 50	
131	Electrolytic	16R 101	
132	Film	CQ 92 1H 103	
133	Electrolytic	16R 101	
134	Film	CQ 92 1H 103	
135		"	
136	Stacking Ceramic	RPE 122C 104Z 50	
137	Film	CQ 92 1H 222	
138		102	
139	Electrolytic	50R 1R0	
140	Stacking Ceramic	RPE 122C 104Z 50	
141	Film	CQ 92 1H 102	
142	Tantal	2.2μF 35V	
143		"	
144	Stacking Ceramic	RPE 122C 104Z 50	
145	Dip Mica	DM 101J	
146	Electrolytic	6.3R 220	
147	Dip Mica	DM 101J	
148		"	
149	Stacking Ceramic	RPE 122C 104Z 50	
150		"	

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 151	Dip Mica	DM 470J	
152		"	
153		561J	
154	Film	CQ 92 1H 103	
155	Dip Mica	DM 470J	
156	Electrolytic	16R 100	
157	Stacking Ceramic	RPE 122C 104Z 50	
158	Dip Mica	DM 680J	
159		"	
160	Electrolytic	16R 100	
161	Stacking Ceramic	RPE 122C 104Z 50	
162	Dip Mica	DM 680J	
163		"	
164		330J	
165	Film	CQ 92 1H 103	
166	Dip Mica	DM 151J	
167	Film	CQ 92 1H 473	
168		102	
169		Deleted	
170	Dip Mica	DM 680J	
171		100J	
172		121J	
173		470J	
174		101J	
175		330J	
176		470J	
177		221J	
178	Stacking Ceramic	RPE 122C 104Z 50	
179	Electrolytic	16R 101	
180		6.3R 221	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 181	Stacking Ceramic	RPE 122C 104Z 50	
182	Electrolytic	6.3R 101	
183	Dip Mica	DM 131J	
184		471J	
185		181J	
186		330J	
187		Deleted	
188		Deleted	
189		Deleted	
190		Deleted	
191	Electrolytic	6.3R 221	
192	Stacking Ceramic	RPE 122C 104Z 50	
193	Film	CQ 92 1H 102	
194	Dip Mica	DM 101J	
195		Deleted	
196	Electrolytic	6.3R 221	
197		Deleted	
198	Electrolytic	16R 221	
199	Stacking Ceramic	RPE 122C 104Z 50	
200	Electrolytic	16R 221	
201	Stacking Ceramic	RPE 122C 104Z 50	
202	Electrolytic	16R 221	
203	Stacking Ceramic	RPE 122C 104Z 50	
204	Electrolytic	16R 221	
205	Stacking Ceramic	RPE 122C 104Z 50	
206		Deleted	
207		Deleted	
208		Deleted	
209		Deleted	
210	Dip Mica	DM 151J	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 211	Dip Mica	DM 220J	
212		330J	
213		470J	
214		499D 104 X 0035A1	
215		Deleted	
216		"	
217		"	
218		"	
219		"	
220		"	
221		"	
222		"	
223		"	
224		"	
225		"	
226		"	
227		"	
228		"	
229		"	
230		"	
231		"	
232		"	
233		"	
234		"	
235		"	
236		"	
237		"	
238		"	
239		"	
240		"	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 241		Deleted	
243		"	
244		"	
245		"	
246		"	
247		"	
248		"	
249		"	
250	Electrolytic	6.3R 221	
251	Stacking Ceramic	RPE 122C 104Z 50	
252	Electrolytic	6.3R 221	
253	Stacking Ceramic	RPE 122C 104Z 50	
254		"	
255		"	
256		"	
257		"	
258		"	
259		"	
260		"	
261		"	
262		"	
263		"	
264		"	
265		"	
266		"	
267		"	
268		"	
269		"	
270		"	

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 271	Stacking Ceramic	RPE 122C 104Z 50	
272		"	
273		"	
274		"	
275		"	
276		"	
277		"	
278		"	
279		"	
280		"	
281		"	
282		"	
283		"	
284		"	
285		"	
286		"	
287		"	
288		"	
289		"	
290		"	
291		Deleted	
292		"	
293		"	
294		"	
295		"	
296		"	
297		"	
298		"	
299		"	
300	Electrolytic	6.3R 221	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 301	Electrolytic	6.3R 221	
302	Stacking Ceramic	RPE 122C 104Z 50	
303		"	
304	Electrolytic	16R 101	
305	Stacking Ceramic	RPE 122C 104Z 50	
306	Electrolytic	16R 101	
307	Stacking Ceramic	RPE 122C 104Z 50	
308		"	
309		"	
310		"	
311		"	
312	Electrolytic	16R 101	
313	Stacking Ceramic	RPE 122C 104Z 50	
314	Electrolytic	16R 101	
315	Stacking Ceramic	RPE 122C 104Z 50	
316		"	
317		"	
318	Electrolytic	16R 101	
319	Stacking Ceramic	RPE 122C 104Z 50	
320		"	
321	Electrolytic	16R 101	
322		"	
323	Stacking Ceramic	RPE 122C 104Z 50	
324		"	
325	Electrolytic	16R 101	
326	Stacking Ceramic	RPE 122C 104Z 50	
327		"	
328		"	
329		"	
330	Electrolytic	16R 101	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 331	Stacking Ceramic	RPE 1220 104Z 50	
332	Electrolytic	16R 101	
333	Stacking Ceramic	RPE 122C 104Z 50	
334	Electrolytic	16R 101	
335		"	
336	Stacking Ceramic	RPE 122C 104Z 50	
337		"	
338	Electrolytic	6.3R 221	
339	Stacking Ceramic	RPE 122C 104Z 50	
340		"	
341	Electrolytic	16R 101	
342	Stacking Ceramic	RPE 122C 104Z 50	
343		"	
344		"	
345		"	
346	Electrolytic	16R 101	
347	Stacking Ceramic	RPE 122C 104Z 50	
348		"	
349	Electrolytic	16R 101	
350	Stacking Ceramic	RPE 122C 104Z 50	
351	Electrolytic	16R 101	
352	Stacking Ceramic	RPE 122C 104Z 50	
353		"	
354		"	
355		"	
356		Deleted	
357	Stacking Ceramic	RPE 122C 104Z 50	
358		"	
359		"	
360		"	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 361	Stacking Ceramic	RPE 122C 104Z 50	
362		"	
363	Electrolytic	16R 101	
364		"	
365	Stacking Ceramic	RPE 122C 104Z 50	
366		"	
367		"	
368		"	
369		"	
370	Electrolytic	16R 101	
371	Stacking Ceramic	RPE 122C 104Z 50	
372	Electrolytic	16R 101	
373	Stakinng Ceramic	RPE 122C 104Z 50	
374		"	
375	Electrolytic	16R 101	
376	Stacking Ceramic	RPE 122C 104Z 50	
377	Electrolytic	16R 101	
378		"	
379	Stacking Ceramic	RPE 122C 104Z 50	
380	Electrolytic	16R 101	
381	Stacking Ceramic	RPE 122C 104Z 50	
382		"	
383		"	
384		"	
385		"	
386		"	
387	Electrolytic	16R 101	
388		Deleted	
389	Electrolytic	16R 101	
390	Stacking Ceramic	RPE 122C 104Z 50	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 391	Stacking Ceramic	RPE 122C 104Z 50	
392		"	
393		"	
394	Stacking Ceramic	RPE 122C 104Z 50	
395		"	
396		"	
397		"	
398		"	
399		"	
400		"	
401		"	
402		"	
403		"	
404	Electrolytic	16R 101	
405	Stacking Ceramic	RPE 122C 104Z 50	
406	Electrolytic	16R 101	
407		"	
408	Stacking Ceramic	RPE 122C 104Z 50	
409	Electrolytic	16R 101	
410	Stacking Ceramic	RPE 122C 104Z 50	
411		"	
412		"	
413		"	
414		"	
415		"	
416		"	
417		"	
418		"	
419		"	
420		"	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 421	Electrolytic	16R 101	
422	Stacking Ceramic	RPE 122C 104Z 50	
423	Electrolytic	16R 101	
424		"	
425		"	
426	Stacking Ceramic	RPE 122C 104Z 50	
427		"	
428		"	
429		"	
430		"	
431		"	
432		"	
433		"	
434		"	
435		"	
436	Electrolytic	16R 101	
437	Stacking Ceramic	RPE 122C 104Z 50	
438	Electrolytic	16R 101	
439		"	
440	Stacking Ceramic	RPE 122C 104Z 50	
441	Electrolytic	16R 101	
442	Stacking Ceramic	RPE 122C 104Z 50	
443		"	
444		"	
445		"	
446		"	
447		"	
448		"	
449		"	
450	Electrolytic	16R 101	

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 451	Stacking Ceramic	RPE 122C 104Z 50	
452	Electrolytic	16R 101	
453		"	
454	Stacking Ceramic	RPE 122C 104Z 50	
455	Electrolytic	16R 101	
456	Stacking Ceramic	RPE 122C 104Z 50	
457		"	
458		"	
459	Electrolytic	16R 101	
460	Stacking Ceramic	RPE 122C 104Z 50	
461	Electrolytic	16R 101	
462	Stacking Ceramic	RPE 122C 104Z 50	
463		"	
464		"	
465		"	
466	Electrolytic	16R 101	
467		"	
468		"	
469	Stacking Ceramic	RPE 122C 104Z 50	
470	Electrolytic	16R 101	
471	Stacking Ceramic	RPE 122C 104Z 50	
472		"	
473		"	
474		"	
475		"	
476	Electrolytic	16R 101	
477		"	
478	Stacking Ceramic	RPE 122C 104Z 50	
479	Electrolytic	16R 101	
480	Stacking Ceramic	RPE 122C 104Z 50	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 481	Electrolytic	16R 101	
482	Stacking Ceramic	RPE 122C 104Z 50	
483	Electrolytic	16R 101	
484	Stacking Ceramic	RPE 122C 104Z 50	
485	Electrolytic	16R 101	
486		6.3R 221	
487	Stacking Ceramic	RPE 122C 104Z 50	
488	Electrolytic	6.3R 221	
489	Stacking Ceramic	RPE 122C 104Z 50	
490		RPE 122C 104Z 50	
491		Deleted	
492	Stacking Ceramic	RPE 122C 104Z 50	
493		"	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
VC 1	Variable Resistor	ECV 1ZW 20 X 53N	
2		"	
3		"	
4		ECV 1ZW 40 X 53N	
5		ECV 1ZW 20 X 53N	
L 1	Inductance	FL 4H 5R 6K	
2		FL 5H 330 K	
3		P-0087	
4		"	
5		FL 4H 5R 6K	
6		FL 5H 270 K	
7		P-0088	
8		P-0086	
9		P-0087	
10		"	
11		"	
12		FL 5H 101 K	
13		" "	
14		" 100 K	
15		" 470 K	
16		" 100 K	
17		" 680 K	
18		" "	
19		" 101 K	
20		FL 4H 3R 3M	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
L 21	Inductance	P-0087	
22		P-0086	
23		P-0075	
24		"	
25		FL 4H 6R 8K	
26		FL 5H 330 K	
27		P-0075	
28		"	
29		"	
30		FL 7H 101 K	
31		" "	
32		" "	
33		" "	
34		" "	
35		" "	
36		P-0075	
37		FL 4H 5R 6K	
38		Deleted	
39		Deleted	
40		FL 9H 100 M	
41		" "	
42		Deleted	
43		FL 9H 100 M	
44		" "	
45		" "	

FA-410N INPUT PROCESSOR BOARD

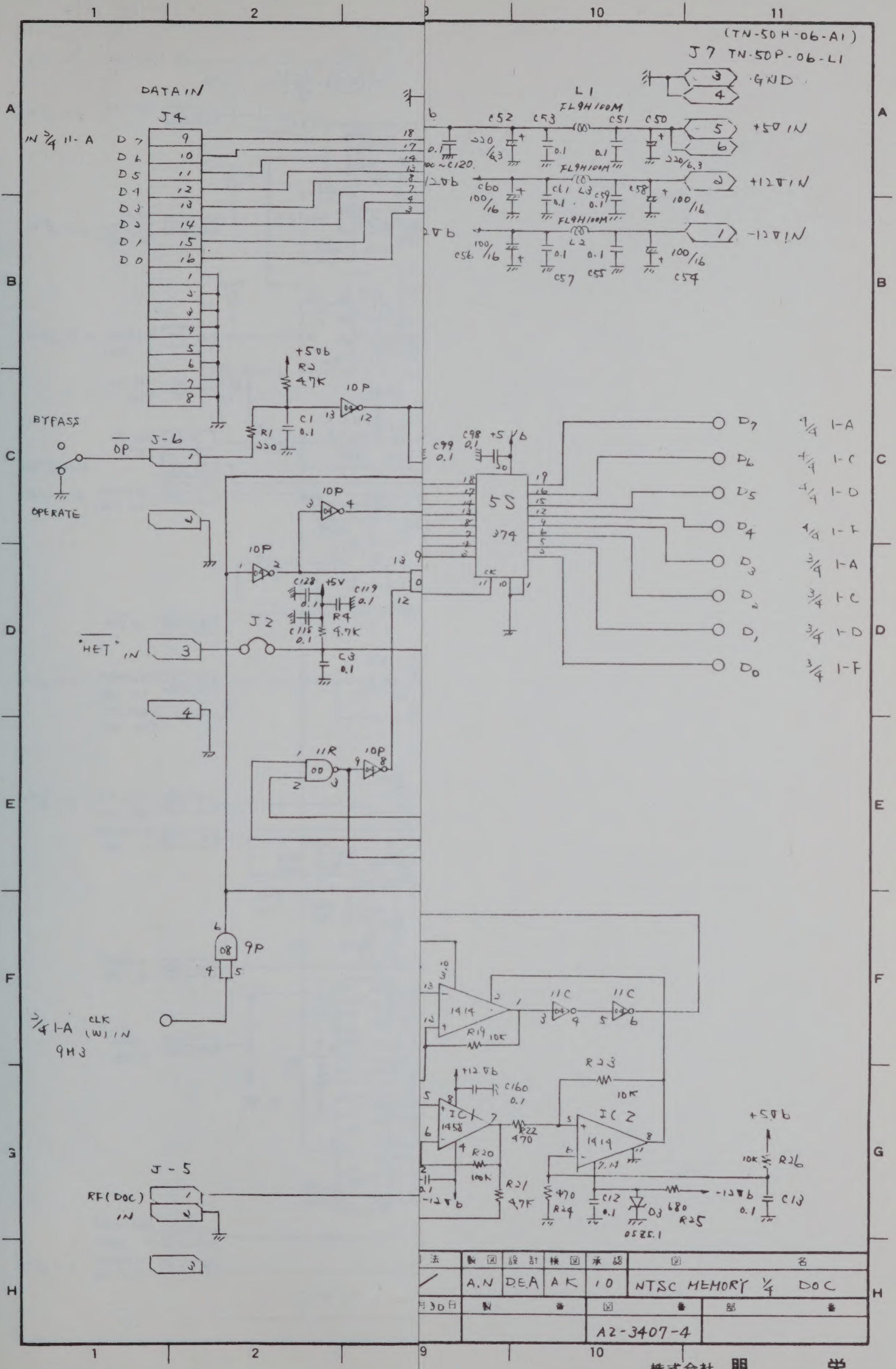
SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
Y 1	Crystal Oschillator	HC 18U 3.579545 MHZ	
DL 1	Delay Line	SDL-300-201T	
SW 1	Switch	S-2030	
TP 1	Test Pin	LC1-S	
2		"	
3		"	
4		"	
5		"	
6		"	
7		"	
8		"	
9		"	
10		"	
11		"	
12		"	
13		"	
14		"	
15		"	
16		"	
17		"	
18		"	
19		"	
20		"	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
TP 21	Test Pin	L01-S	
22		"	
23		"	
24		"	
25		Deleted	
26		"	
27		"	
28		"	
29		"	
30		PTR-45-115	
31		"	
32		"	
33		"	
34		"	
35		"	
36		"	
37		"	
38		"	
39		"	
40		"	
41		"	
42		"	
43		"	
44		LC1-S	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
J 1	Connector	TL-G-15-S3T2-E	
2		-12-	
3		-03-	
4		-04-	
5		-06-	
6		-08-	
7		IC-31-14	
	Plate	for IC-31-14	
J 8	Connector	IC-31-14	
	Plate	for IC-31-14	
J 9	Connector	IL-G-07-S3T2-E	
10		TN50P-06-L1	
11		"	
12		TN50P-04-L1	
	Printed Circuit Board	A2-3488	
		3489	
		3490	
		3491	
		3492	


(TN-50H-06-A1)
J7 TN-50P-06-L1
GND
+5V IN
+12V IN
-12V IN
L1 FL9H100M
L2
L3
C52 C53 C51 C50
220/6.3
C60 C61 C59 C58
100/16
C56 C57 C55 C54
DATA IN
J4
IN 3/4 11-A
D7 D6 D5 D4 D3 D2 D1 D0
+5V R2 4.7K
10P
C1 0.1
R1 220
BYPASS
OPERATE
OP
J-6
C99 0.1
C98 0.1 +5V
5S
374
CK
D7 4/4 1-A
D6 4/4 1-C
D5 4/4 1-D
D4 4/4 1-F
D3 3/4 1-A
D2 3/4 1-C
D1 3/4 1-D
D0 3/4 1-F
C128 +5V C119 0.1
C115 0.1 R4 4.7K
J2
C3 0.1
"HET" IN
11R
08 9P
3/4 1-A CLK (W) IN
9H3
1414
R19 10K
11C
R23 10K
IC1 1458
+12V C160 0.1
R22 470
IC2 1414
R20 100K
R21 4.7K
R24 470
C12 0.1
D3 05Z5.1
R25 680
-12V
+5V
R26 10K
C13 0.1
J-5
RF(DOC) IN

法	製図	設計	検図	承認	図	名
/	A.N	D.E.A	A K	1 0	NTSC MEMORY 1/4 DOC	
月30日	製	番	図	番	部	番
			A2-3407-4			

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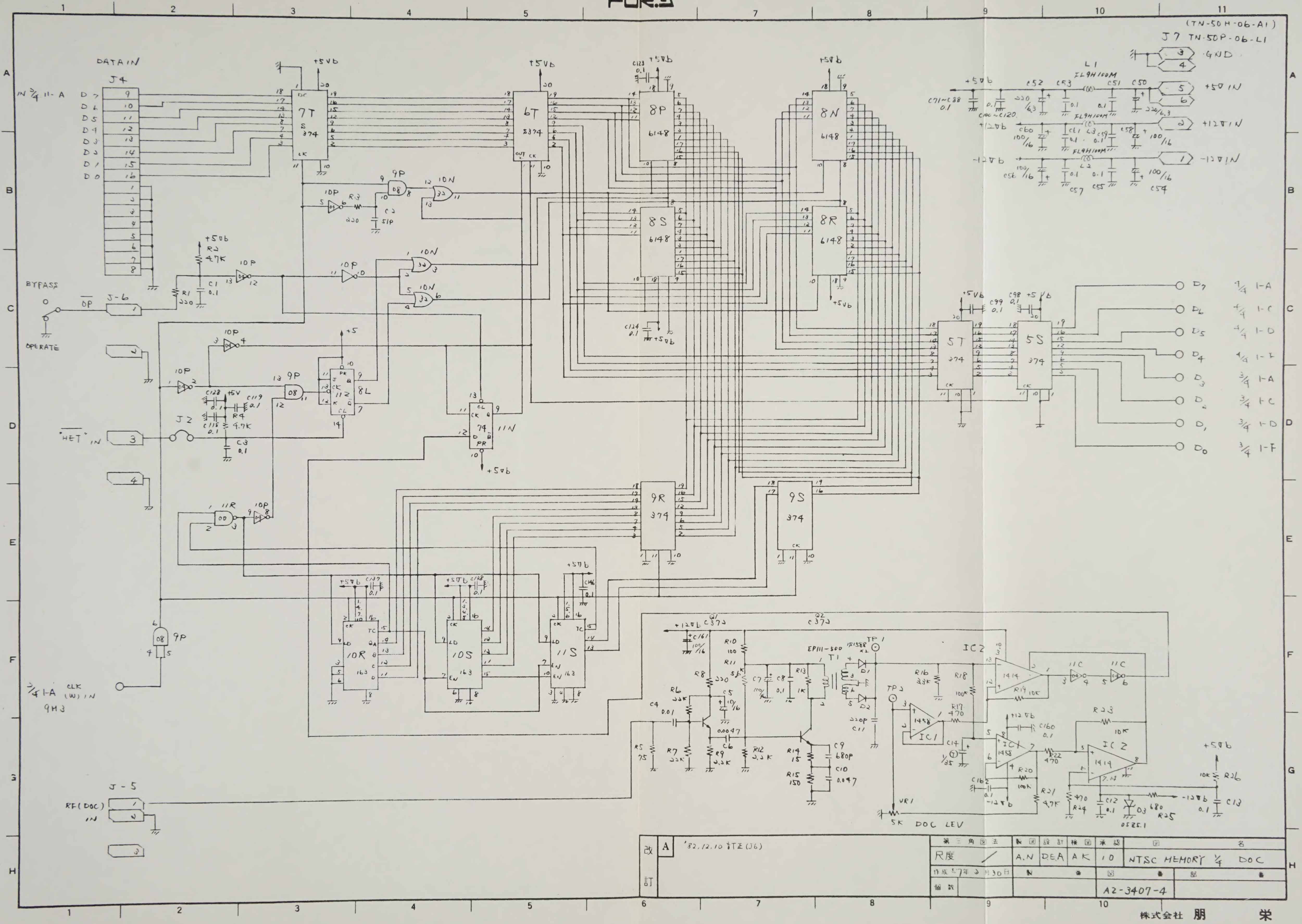
FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
J 1	Connector	TL-G-15-S3T2-E	
2		-12-	
3		-03-	
4		-04-	
5		-06-	
6		-08-	
7		IC-31-14	
	Plate	for IC-31-14	
J 8	Connector	IC-31-14	
	Plate	for IC-31-14	
J 9	Connector	IL-G-07-S3T2-E	
10		TN50P-06-L1	
11		"	
12		TN50P-04-L1	
	Printed Circuit Board	A2-3488	
		3489	
		3490	
		3491	
		3492	

FOR.A


(TN-50H-06-A1)
J7 TN-50P-06-L1
GND
+5V IN
+12V IN
-12V IN
DATA IN
J4
IN 3/4 II-A
D7
D6
D5
D4
D3
D2
D1
D0
BYPASS
OPERATE
OP
J-6
"HET" IN
J2
3/4 I-A CLK (W) IN
9H3
J-5
RF(DOC) IN
7T S374
6T S374
8P 6148
8N 6148
8S 6148
8R 6148
8L 112
11N 74
9R 374
9S 374
5T 374
5S 374
10R 163
10S 163
11S 163
9P
10N
10P
11R
11C
IC1 1458
IC2 1414
Q1 C372
Q2 C372
T1 EP111-300
TP1
TP2
VR1 5K DOC LEV
D7 4/4 I-A
D6 4/4 I-C
D5 4/4 I-D
D4 4/4 I-F
D3 3/4 I-A
D2 3/4 I-C
D1 3/4 I-D
D0 3/4 I-F
+5Vb
+12Vb
-12Vb
L1 FL9H100M
L2
L3

改訂	A	'82.12.10 訂正(J6)

第三角図法	製図	設計	検図	承認	図名
尺度 /	A.N	DEA	AK	10	NTSC MEMORY 1/4 DOC
作成 57年 3月30日	製番		図番		部番
個数			A2-3407-4		

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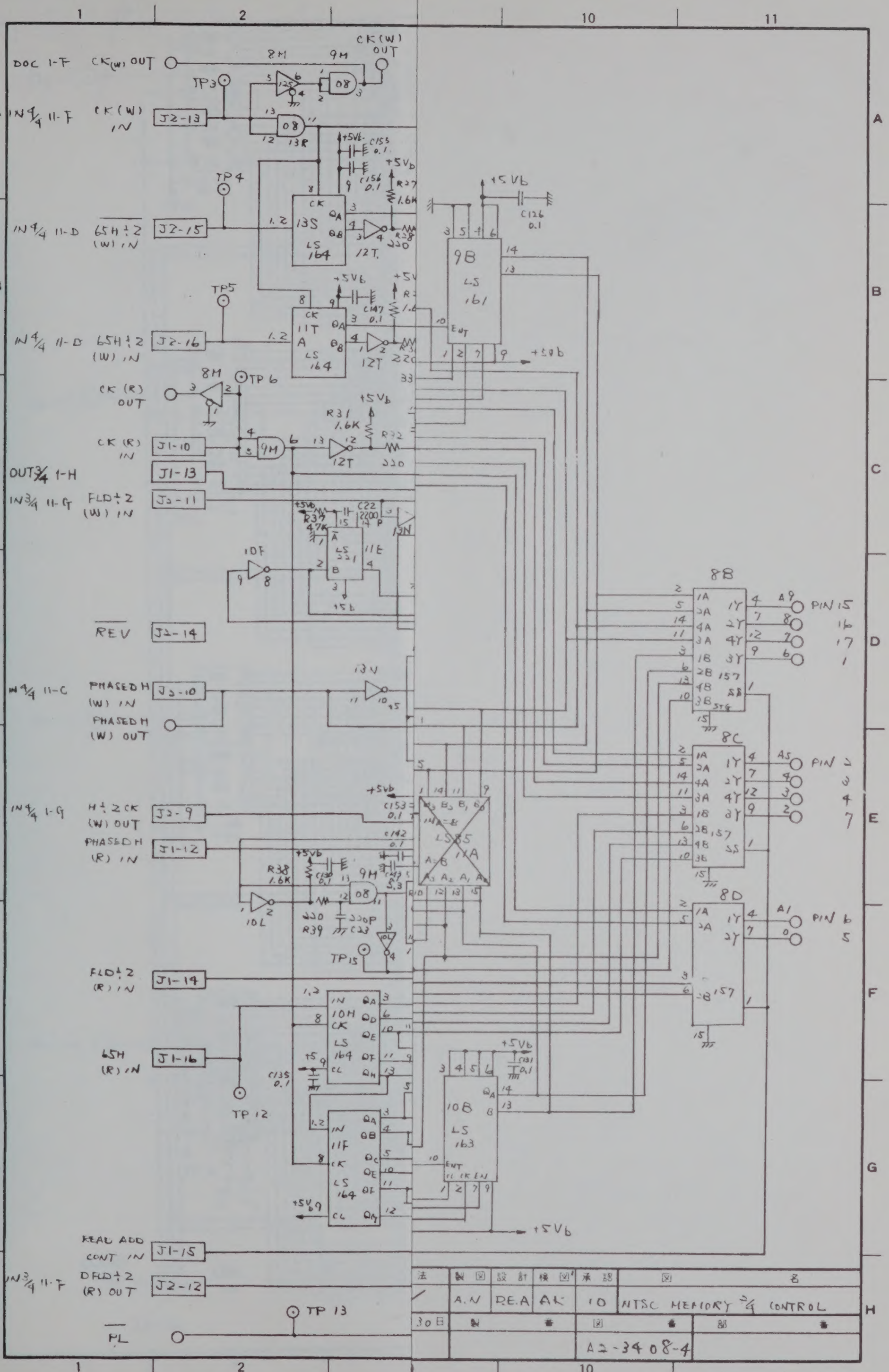
DOC 1-F CK(W) OUT
CK(W) OUT
8M
9M
08
TP3
IN 4/4 11-F CK(W) IN J2-13
13R
+5Vb C155 0.1
C156 0.1
R27 1.6K
TP4
IN 4/4 11-D 65H÷2 (W) IN J2-15
CK 13S LS 164 QA QB
12T
R28 220
+5Vb C126 0.1
9B LS 161 ENT
TP5
IN 4/4 11-D 65H÷2 (W) IN J2-16
CK 11T A LS 164 QA QB
C147 0.1
R30 220
+5Vb
8M TP6
CK (R) OUT
R31 1.6K R32
CK (R) IN J1-10
9M
12T 220
OUT 3/4 1-H J1-13
IN 3/4 11-G FLD÷2 (W) IN J2-11
+5Vb R37 47K C22 2200P
LS 221 11E
13N
10F
REV J2-14
8B
1A 2A 4A 3A 1B 2B 4B 3B 157 STB SB
1Y 2Y 4Y 3Y
A9 PIN 15
8 16
7 17
6 1
IN 4/4 11-C PHASED H (W) IN J2-10
PHASED H (W) OUT
13V
8C
A5 PIN 2
4 3
3 4
2 7
IN 4/4 1-G H÷2 CK (W) OUT J2-9
+5Vb C153 0.1
C142 0.1
LS85 A=B A>B
PHASED H (R) IN J1-12
R38 1.6K
C130 0.1
9M 08
220 R39
330P C23
10L
TP15
8D
A1 PIN 6
0 5
FLD÷2 (R) IN J1-14
IN CK LS 164 CL QA QD QE QF QH 10H
+5Vb C131 0.1
65H (R) IN J1-16
C135 0.1
TP12
108 LS 163 QA QB ENT
IN CK LS 164 CL QA QB QC QE QF QH 11F
+5Vb
READ ADD CONT IN J1-15
IN 3/4 11-F DFLD÷2 (R) OUT J2-12
TP13
PL
1 2 10 11
A B C D E F G H

法	製図	設計	検図	承認	図	名
/	A.N	RE.A	AK	10	NTSC MEMORY 3/4 CONTROL	
30日				図番	A2-3408-4	

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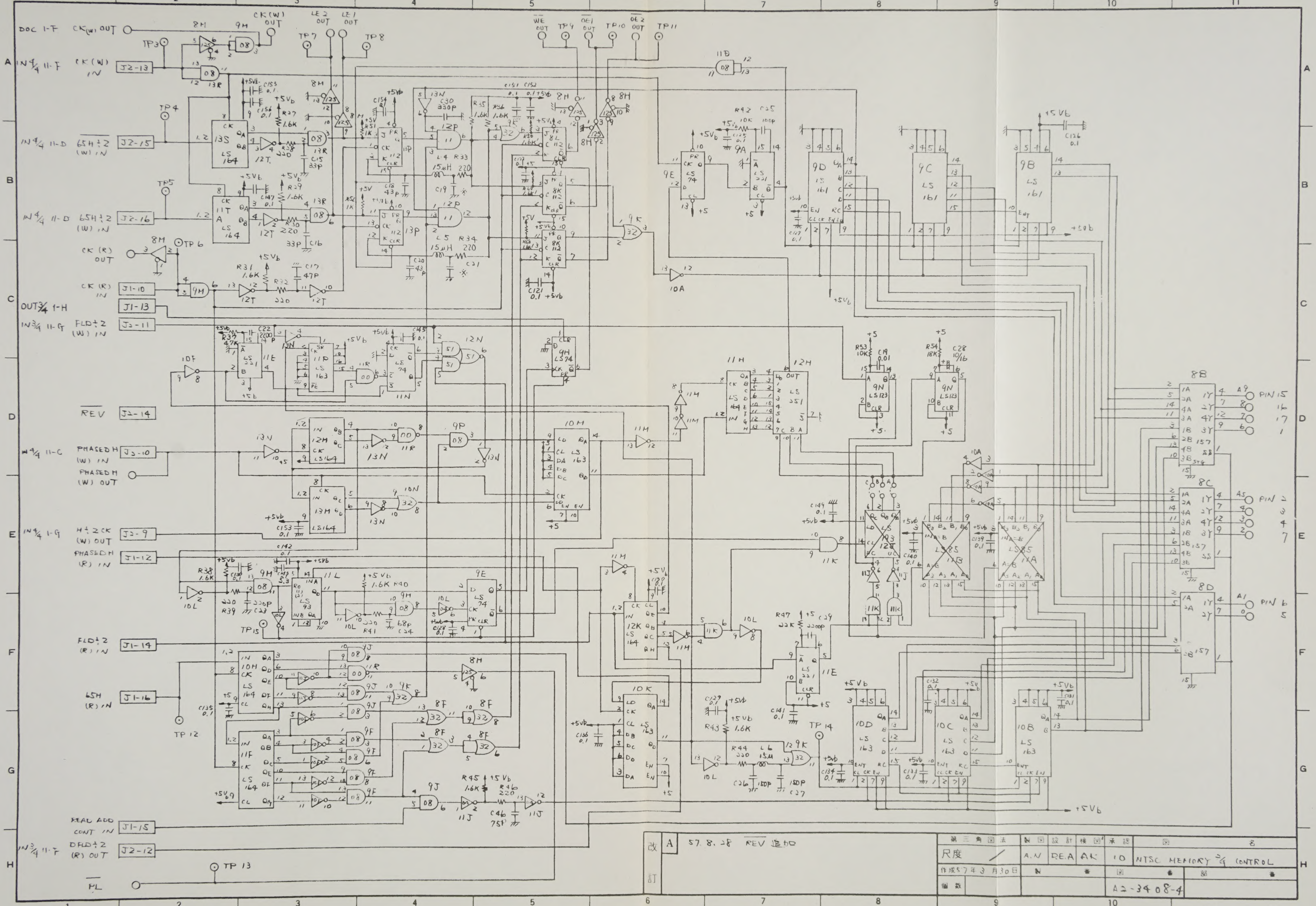
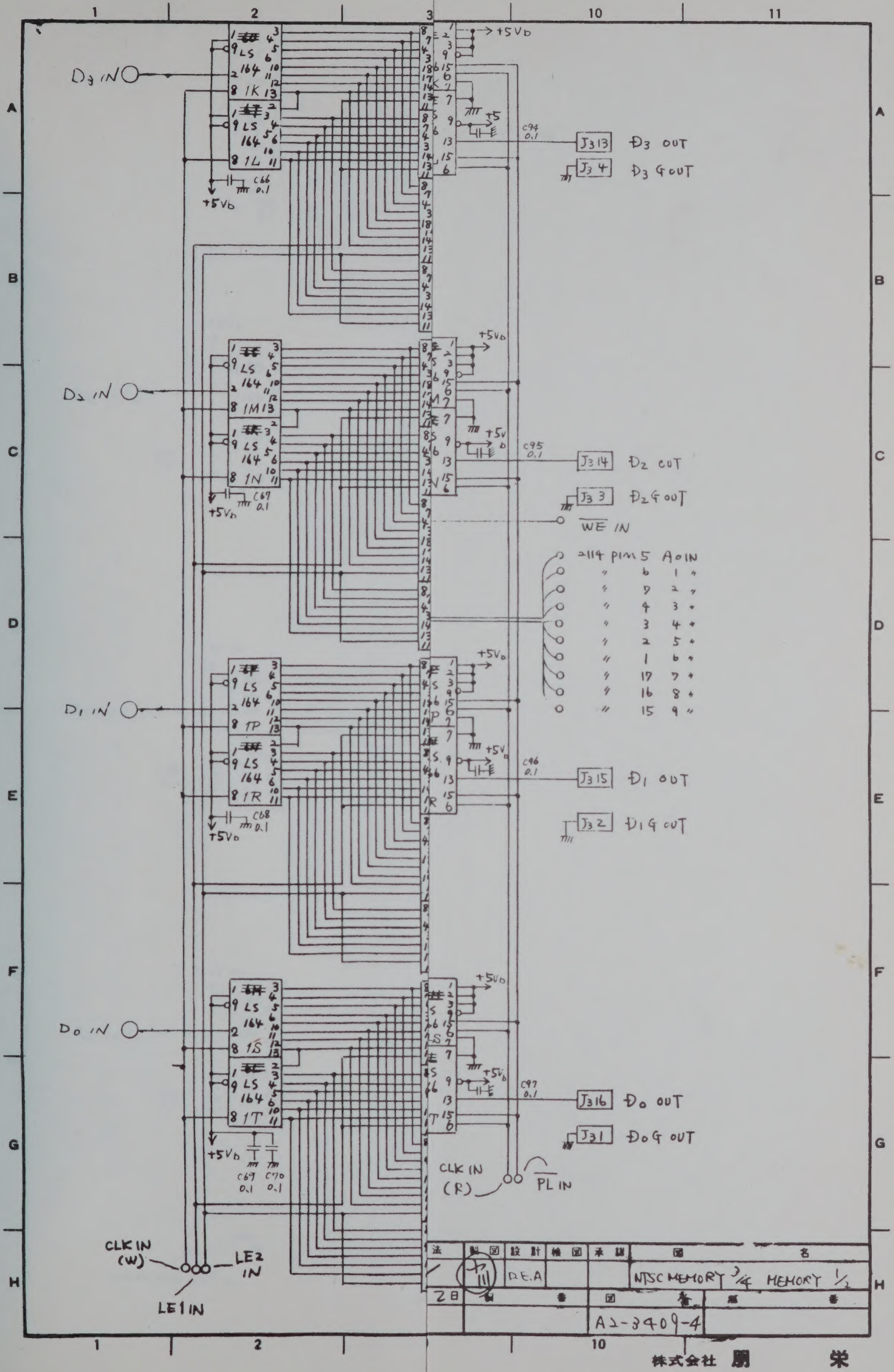
FOR.A


DOC 1-F CK(W) OUT
IN 4/4 11-F CK(W) IN J2-13
IN 4/4 11-D 65H÷2 (W) IN J2-15
IN 4/4 11-D 65H÷2 (W) IN J2-16
CK(R) OUT
CK(R) IN J1-10
OUT 3/4 1-H J1-13
IN 3/4 11-G FLD÷2 (W) IN J2-11
REV J2-14
IN 4/4 11-C PHASED H (W) IN J3-10
PHASED H (W) OUT
IN 4/4 1-G H÷2CK (W) OUT J2-9
PHASED H (R) IN J1-12
FLD÷2 (R) IN J1-14
65H (R) IN J1-16
READ ADD CONT IN J1-15
IN 3/4 11-F DFLD÷2 (R) OUT J2-12
FL
CK(W) OUT
LE2 OUT
LE1 OUT
WE OUT
OE1 OUT
OE2 OUT
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP11
TP12
TP13
TP14
TP15
13S LS164
11T LS164
12P LS112
13P LS112
8L LS112
8K LS112
9A LS221
9E LS74
9D LS161
9C LS161
9B LS161
11E LS221
11P LS163
11N LS74
9H LS74
11H LS164
12H LS351
9N LS123
12M LS164
13M LS164
10M LS163
11L LS93
9E LS74
12K LS164
10H LS164
11F LS164
10K LS163
11E LS221
10D LS163
10C LS163
10B LS163
12B LS193
11B LS85
11A LS85
8B 157
8C 157
8D 157
A9 PIN 15
16
17
1
A5 PIN 2
3
4
7
A1 PIN 6
5
+5Vb

改訂	A	57. 8. 28 REV 追加

第三角図法	製図	設計	検図	承認	図名
尺度 /	A.N	DE.A	AK	10	NTSC MEMORY 2/4 CONTROL
作成57年3月30日	製番			図番	部番
個数				A2-3408-4	

株式会社 朋栄

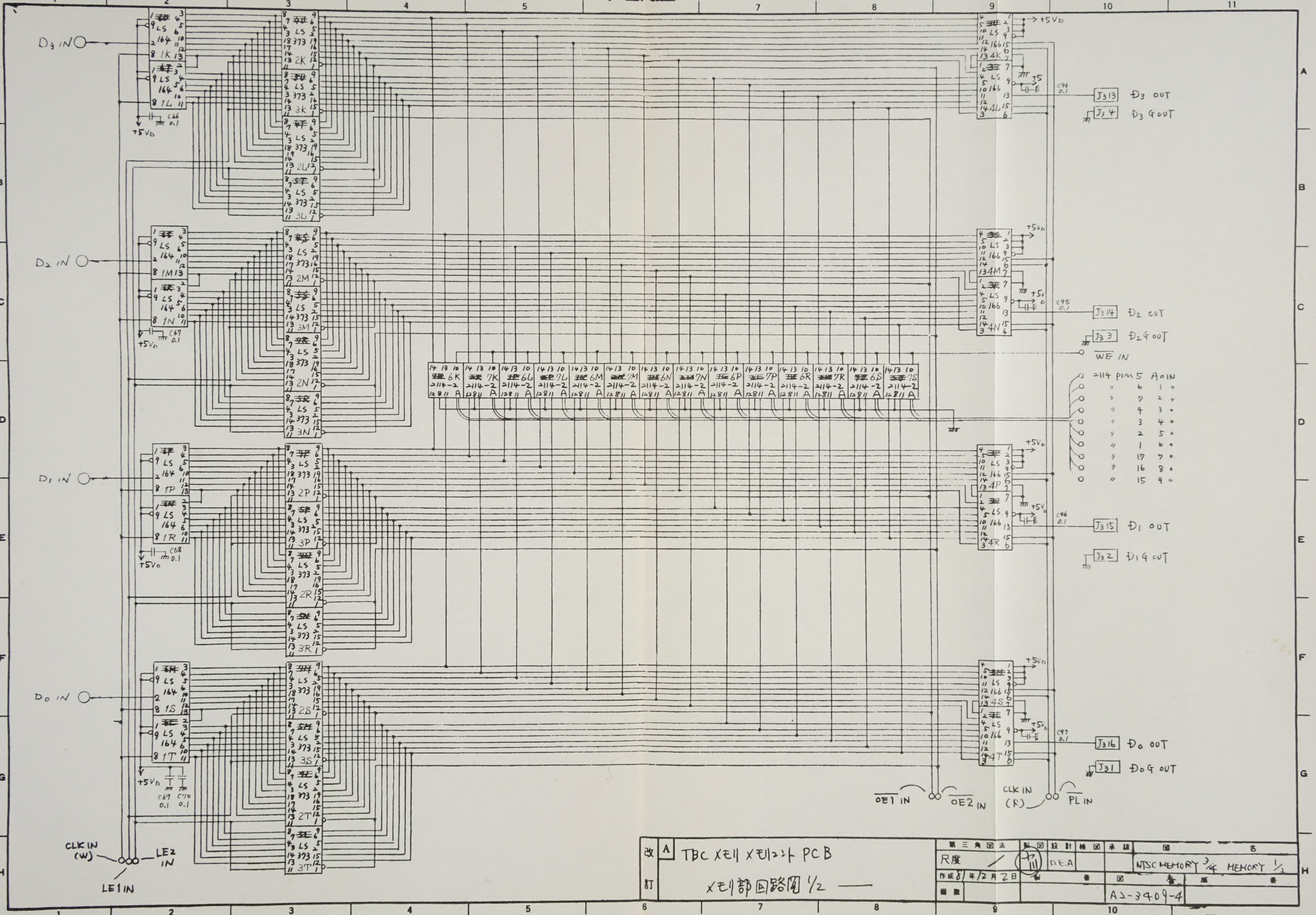


1
2
3
10
11
A
B
C
D
E
F
G
H
D3 IN
LS 164 1K
LS 164 1L
C66 0.1
+5VD
K
L
+5VD
+5
C94 0.1
J3 13
D3 OUT
J3 4
D3 G OUT
D2 IN
LS 164 1M
LS 164 1N
C67 0.1
+5VD
M
N
+5V
C95 0.1
J3 14
D2 OUT
J3 3
D2 G OUT
$\overline{\text{WE}}$ IN
2114 PIN 5 A0 IN
〃 6 1 〃
〃 7 2 〃
〃 4 3 〃
〃 3 4 〃
〃 2 5 〃
〃 1 6 〃
〃 17 7 〃
〃 16 8 〃
〃 15 9 〃
D1 IN
LS 164 1P
LS 164 1R
C68 0.1
+5VD
P
R
+5VD
+5VD
C96 0.1
J3 15
D1 OUT
J3 2
D1 G OUT
D0 IN
LS 164 1S
LS 164 1T
C69 0.1
C70 0.1
+5VD
S
T
+5VD
+5VD
C97 0.1
J3 16
D0 OUT
J3 1
D0 G OUT
CLK IN (R)
$\overline{\text{PL}}$ IN
CLK IN (W)
LE2 IN
LE1 IN

法	製図	設計	検図	承認	図名
/	和	D.E.A			NTSC MEMORY 3/4 MEMORY 1/2
2B	製番		図番		原番
			A2-3409-4		

株式会社 朋栄

FOR.A


D3 IN
D2 IN
D1 IN
D0 IN
1K
1L
2K
3K
2L
3L
1M
1N
2M
3M
2N
3N
1P
1R
2P
3P
2R
3R
1S
1T
2S
3S
2T
3T
LS 164
LS 373
LS 166
4K
4L
4M
4N
4P
4R
4S
4T
6K
7K
6L
7L
6M
7M
6N
7N
6P
7P
6R
7R
6S
7S
2114-2
+5VD
C66 0.1
C67 0.1
C68 0.1
C69 0.1
C70 0.1
C94 0.1
C95 0.1
C96 0.1
C97 0.1
J3 13 D3 OUT
J3 4 D3 G OUT
J3 14 D2 OUT
J3 3 D2 G OUT
J3 15 D1 OUT
J3 2 D1 G OUT
J3 16 D0 OUT
J3 1 D0 G OUT
WE IN
2114 PIN 5 A0 IN
〃 6 1 〃
〃 7 2 〃
〃 4 3 〃
〃 3 4 〃
〃 2 5 〃
〃 1 6 〃
〃 17 7 〃
〃 16 8 〃
〃 15 9 〃
OE1 IN
OE2 IN
CLK IN (R)
PL IN
CLK IN (W)
LE2 IN
LE1 IN

改訂 A

TBC メモリ メモリユニット PCB

メモリ部回路図 1/2 ——

第三角図法

尺度 /

製図 設計 検図 承認

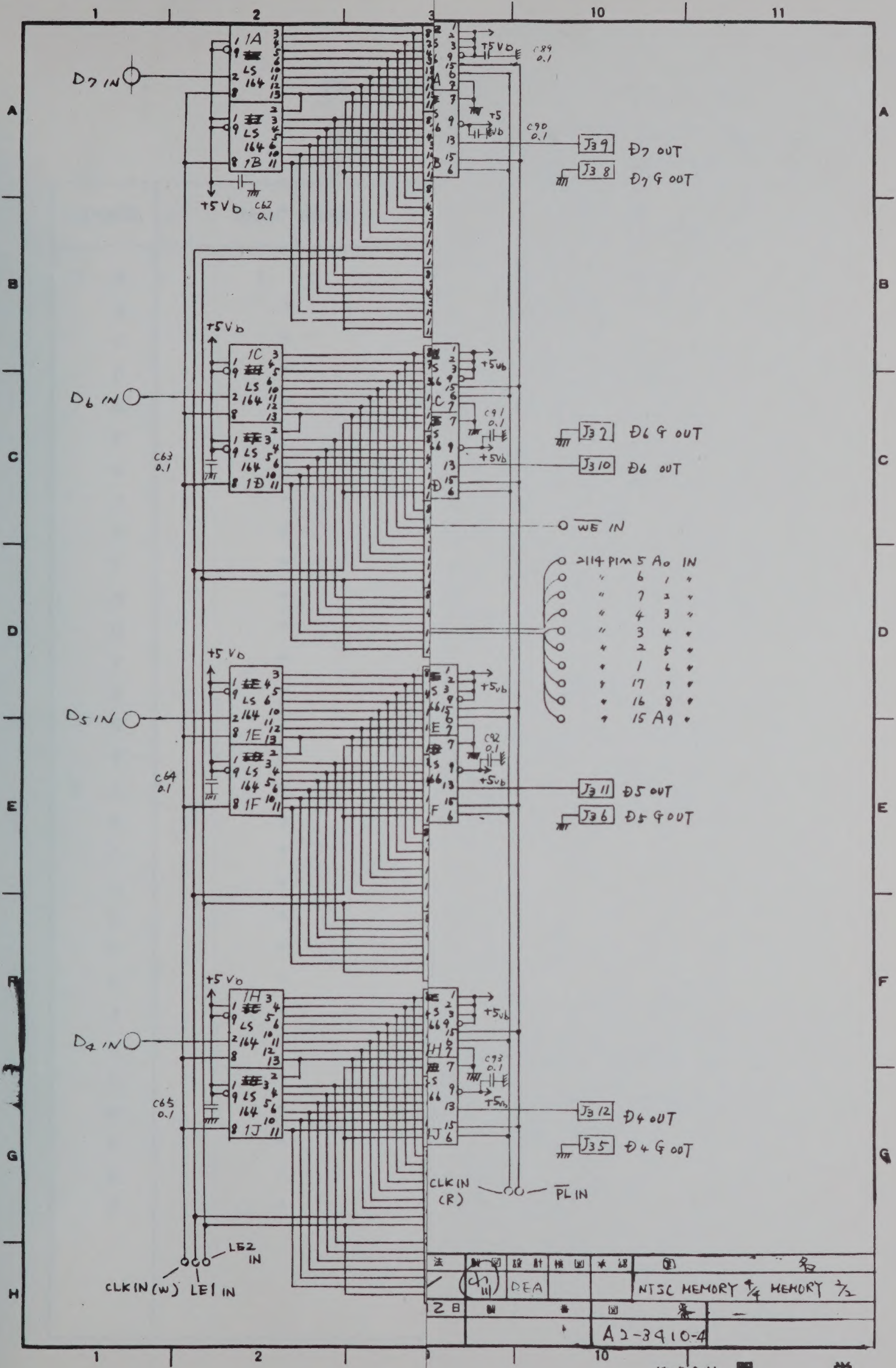
D.E.A

作成 81年12月2日

図名 NTSC MEMORY 3/4 MEMORY 1/2

図番 A2-3409-4

株式会社 朋栄


D7 IN
1A
LS 164
1B
+5Vb
C62 0.1
C89 0.1
C90 0.1
J3 9 D7 OUT
J3 8 D7 G OUT
D6 IN
1C
LS 164
1D
C63 0.1
C91 0.1
J3 7 D6 G OUT
J3 10 D6 OUT
WE IN
2114 PIN 5 A0 IN
〃 6 1 〃
〃 7 2 〃
〃 4 3 〃
〃 3 4 〃
〃 2 5 〃
〃 1 6 〃
〃 17 7 〃
〃 16 8 〃
〃 15 A9 〃
D5 IN
1E
LS 164
1F
C64 0.1
C92 0.1
J3 11 D5 OUT
J3 6 D5 G OUT
D4 IN
1H
LS 164
1J
C65 0.1
C93 0.1
J3 12 D4 OUT
J3 5 D4 G OUT
CLK IN (R)
PL IN
CLK IN (W)
LE1 IN
LE2 IN
製図
設計
検図
承認
図名
DEA
NTSC MEMORY 1/4 MEMORY 2/2
図番
A2-3410-4

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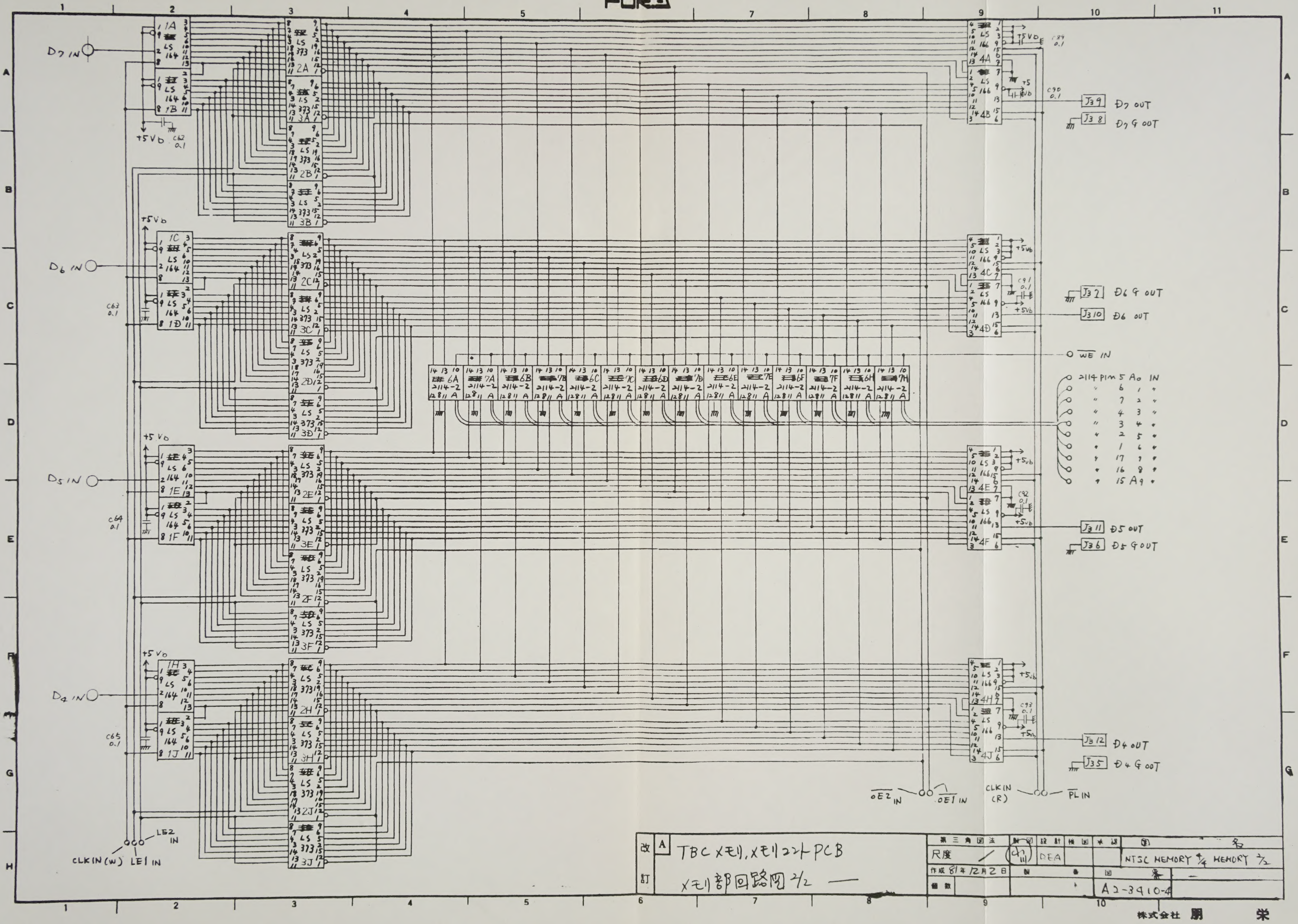
FOR.A


D7 IN
D6 IN
D5 IN
D4 IN
1A LS 164
1B LS 164
1C LS 164
1D
1E LS 164
1F LS 164
1H LS 164
1J LS 164
2A LS 373
3A LS 373
2B LS 373
3B LS 373
2C LS 373
3C LS 373
2D LS 373
3D LS 373
2E LS 373
3E LS 373
2F LS 373
3F LS 373
2H LS 373
3H LS 373
2J LS 373
3J LS 373
6A 2114-2
7A 2114-2
6B 2114-2
7B 2114-2
6C 2114-2
7C 2114-2
6D 2114-2
7D 2114-2
6E 2114-2
7E 2114-2
6F 2114-2
7F 2114-2
6H 2114-2
7H 2114-2
4A LS 166
4B LS 166
4C LS 166
4D LS 166
4E LS 166
4F LS 166
4H LS 166
4J LS 166
+5Vb
C62 0.1
C63 0.1
C64 0.1
C65 0.1
C89 0.1
C90 0.1
C91 0.1
C92 0.1
C93 0.1
J3 9 D7 OUT
J3 8 D7 G OUT
J3 7 D6 G OUT
J3 10 D6 OUT
J3 11 D5 OUT
J3 6 D5 G OUT
J3 12 D4 OUT
J3 5 D4 G OUT
WE IN
2114 PIN 5 A0 IN
" 6 1 "
" 7 2 "
" 4 3 "
" 3 4 "
" 2 5 "
" 1 6 "
" 17 7 "
" 16 8 "
" 15 A9 "
OE2 IN
OE1 IN
CLK IN (R)
PL IN
CLK IN (W)
LE1 IN
LE2 IN
1 2 3 4 5 6 7 8 9 10 11
A B C D E F G H

改訂	A	TBCメモリ, メモリユニットPCB メモリ部回路図 2/2 —

第三角図法	製図	設計	検図	承認	図名
尺度 /	(ｲﾁ)	DEA			NTSC MEMORY 4/4 MEMORY 2/2
作成 81年12月2日	製番		図番		—
個数			A2-3910-4		

株式会社 朋栄

FA-410N MEMORY BOARD

A2-3407-1~3410-1

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
1 A	I C	SN 74 LS 164	
B	"	"	
C	"	"	
D	"	"	
E	"	"	
F	"	"	
H	"	"	
J	"	"	
K	"	"	
L	"	"	
M	"	"	
N	"	"	
P	"	"	
R	"	"	
S	"	"	
T	"	"	
2 A	"	SN 74 LS 373	
B	"	"	
C	"	"	
D	"	"	
E	"	"	
F	"	"	
H	"	"	
J	"	"	
K	"	"	
L	"	"	
M	"	"	
N	"	"	
P	"	"	
R	"	"	

FA-410N MEMORY BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
2 S	I C	SN 74 LS 373	
T	"	"	
3 A	"	"	
B	"	"	
C	"	"	
D	"	"	
E	"	"	
F	"	"	
H	"	"	
J	"	"	
K	"	"	
L	"	"	
M	"	"	
N	"	"	
P	"	"	
R	"	"	
S	"	"	
T	"	"	
4 A	"	SN 74 LS 166	
B	"	"	
C	"	"	
D	"	"	
E	"	"	
F	"	"	
H	"	"	
J	"	"	
K	"	"	
L	"	"	
M	"	"	
N	"	"	

FA-410N MEMORY BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
4 P	I C	SN 74 LS 166	
R	"	"	
S	"	"	
T	"	"	
5 S	"	SN 74 LS 374	
T	"	"	
6 A	"	HM 472114-2	
B	"	"	
C	"	"	
D	"	"	
E	"	"	
F	"	"	
H	"	"	
J	"	"	
K	"	"	
L	"	"	
M	"	"	
N	"	"	
P	"	"	
R	"	"	
S	"	"	
T	"	SN 74 LS 374	
7 A	"	HM 472114-2	
B	"	"	
C	"	"	
D	"	"	
E	"	"	
F	"	"	
H	"	"	
J	"	"	
K	"	"	
L	"	"	

FA-410N MEMORY BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
7 M	I C	HM 472114-2	
N	"	"	
P	"	"	
R	"	"	
S	"	"	
T	"	SN 74 LS 374	
8 B	"	SN 74 LS 157	
C	"	"	
D	"	"	
F	"	SN 74 LS 32	
H	"	SN 74 LS 125	
K	"	SN 74 LS 112	
L	"	"	
M	"	SN 74 LS 125	
N	"	HM 6148 P	
P	"	"	
R	"	"	
S	"	"	
9 A	"	SN 74 LS 221	
B	"	SN 74 LS 161	
C	"	"	
D	"	"	
E	"	SN 74 LS 74	
F	"	SN 74 LS 08	
J	"	"	
K	"	SN 74 LS 32	
M	"	SN 74 LS 08	
P	"	"	
R	"	SN 74 LS 374	
S	"	"	
H	"	SN 74 LS 74A	
N	"	SN 74 LS 123	

FA-410N MEMORY BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
10 A	I C	SN 74 LS 04	
B	"	SN 74 LS 163	
C	"	"	
D	"	"	
F	"	SN 74 LS 04	
H	"	SN 74 LS 164	
K	"	SN 74 LS 163	
L	"	SN 74 LS 04	
M	"	SN 74 LS 163	
N	"	SN 74 LS 32	
P	"	SH 74 LS 04	
R	"	SN 74 LS 163	
S	"	"	
11 A	"	Deleted	
B	"	"	
C	"	SN 74 LS 04	
D	"	SN 74 LS 08	
E	"	SN 74 LS 221	
F	"	SN 74 LS 164	
H	"	"	
J	"	SN 74 LS 04	
K	"	SN 74 LS 08	
L	"	SN 74 LS 93	
M	"	SN 74 LS 04	
N	"	SN 74 LS 74	
P	"	SN 74 LS 163	
R	"	SN 74 LS 00	
S	"	SN 74 LS 163	
T	"	SN 74 LS 164	

FA-410N MEMORY BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
12 H	I C	SN 74 LS 251	
J	"	Deleted	
K	"	SN 74 LS 164	
M	"	SN 74 LS 164	
N	"	SN 74 LS 51	
P	"	SN 74 LS 11	
T	"	SN 74 LS 04	
M	"	SN 74 LS 164	
N	"	SN 74 LS 04	
P	"	SN 74 LS 112	
R	"	SN 74 LS 08	
S	"	SN 74 LS 164	
IC 1	I C	MC 1458 P 1	
2	"	MC 1414 P	
Q 1	Transistor	2 SC 372	
2	"	"	
D 1	Diode	IS 1588	
2	"	"	
3	Zener	05Z 5.1	

SYMBOL	PART NAME	DESCRIPTIONS		REMARKS
R 1	Fixed Resistor	CR 25JU	221	
2	"	"	472	
3	"	"	221	
4	"	"	472	
5	"	"	750	
6	"	"	223	
7	"	"	223	
8	"	"	221	
9	"	"	222	
10	"	"	101	
11	"	"	562	
12	"	"	222	
13	"	"	102	
14	"	"	150	
15	"	"	151	
16	"	"	332	
17	"	"	471	
18	"	"	104	
19	"	"	103	
20	"	"	104	
21	"	"	472	
22	"	"	471	
23	"	"	103	
24	"	"	471	
25	"	"	681	
26	"	"	103	
27	"	"	162	
28	"	"	221	
29	"	"	162	
30	"	"	221	

FA-410N MEMORY BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
R 31	Fixed Resistor	CR 25JU 162	
32	"	" 221	
33	"	" "	
34	"	" "	
35	"	" 162	
36	"	" "	
37	"	" 473	
38	"	" 162	
39	"	" 221	
40	"	" 162	
41	"	" 221	
42	"	" 103	
43	"	" 162	
44	"	" 221	
45	"	" 162	
46	"	" 221	
47	"	" 223	
48	"	" 162	
49	"	" "	
50	"	" "	
51	"	" "	
52	"	" "	
53	"	" 103	
4	"	" 183	
VR 1	Variable Resistor	GFP-06 502	

FA-410N MEMORY BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 1	Ceramic	104Z	
2	Dip Mica	DM 510J	
3	Ceramic	104Z	
4	Film	CQ 92 1H 103	
5	Electrolytic	16R 100	
6	Film	CQ 92 1H 472	
7	Electrolytic	16T 101	
8	Ceramic	104Z	
9	Dip Mica	DM 680J	
10	Film	CQ 92 1H 473	
11	Dip Mica	DM 221J	
12	Ceramic	104Z	
13	"	"	
14	Tantal	1μF 35V	
15	Dip Mica	DM 330J	
16	"	" "	
17	"	" 470J	
18	"	" 300J	
19	Film	CQD 921H 0.01U	
20	Dip Mica	DM 300J	
21	Deleted		
22	Film	CQ 92 1H 222	
23	Dip Mica	DM 221J	
24	"	" 680J	
25	"	" 101J	
26	"	" 151J	
27	"	" "	
28	Electrolytic	ECEBICS 100	
29	Film	CQ 92 1H 222	
30	Dip Mica	DM 331J	

FA-410N MEMORY BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 31	Deleted		
32	"		
33	"		
34	"		
35	"		
36	"		
37	"		
38	"		
39	"		
40	"		
41	"		
42	"		
43	"		
44	"		
45	"		
46	Dip Mica	DM 750J	
47	Deleted		
48	"		
49	"		
50	Electrolytic	6.3T 221	
51	Ceramic	104Z	
52	Electrolytic	6.3T 221	
53	Ceramic	104Z	
54	Electrolytic	16T 101	
55	Ceramic	104Z	
56	Electrolytic	16T 101	
57	Ceramic	104Z	
58	Electrolytic	16T 101	
59	Ceramic	104Z	
60	Electrolytic	16T 101	

FA-410N MEMORY BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 61	Ceramic	104Z	
62	"	"	
63	"	"	
64	"	"	
65	"	"	
66	"	"	
67	"	"	
68	"	"	
69	"	"	
70	"	"	
71	"	"	
72	"	"	
73	"	"	
74	"	"	
75	"	"	
76	"	"	
77	"	"	
78	"	"	
79	"	"	
80	"	"	
81	"	"	
82	"	"	
83	"	"	
84	"	"	
85	"	"	
86	"	"	
87	"	"	
88	"	"	
89	"	"	
90	"	"	

FA-410N MEMORY BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 91	Ceramic	104Z	
92	"	"	
93	"	"	
94	"	"	
95	"	"	
96	"	"	
97	"	"	
98	"	"	
99	"	"	
100	"	"	
101	"	"	
102	"	"	
103	"	"	
104	"	"	
105	"	"	
106	"	"	
107	"	"	
108	"	"	
109	"	"	
110	"	"	
111	"	"	
112	"	"	
113	"	"	
114	"	"	
115	"	"	
116	"	"	
117	"	"	
118	"	"	
119	"	"	
120	"	"	

FA-410N MEMORY BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 121	Ceramic	104Z	
122	"	"	
123	"	"	
124	"	"	
125	"	"	
126	"	"	
127	"	"	
128	"	"	
129	"	"	
130	"	"	
131	"	"	
132	"	"	
133	"	"	
134	"	"	
135	"	"	
136	"	"	
137	"	"	
138	"	"	
139	"	"	
140	"	"	
141	"	"	
142	"	"	
143	"	"	
144	Deleted		
145	Ceramic	104Z	
146	"	"	
147	"	"	
148	Deleted		
149	Ceramic	104Z	
150	"	"	

FA-410N MEMORY BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 151	Ceramic	104Z	
152	"	"	
153	"	"	
154	"	"	
155	"	"	
156	"	"	
157	Deleted		
158	"		
159	"		
160	Ceramic	104Z	
161	Electrolytic	16T 101	
162	Ceramic	104Z	

FA-410N MEMORY BOARD

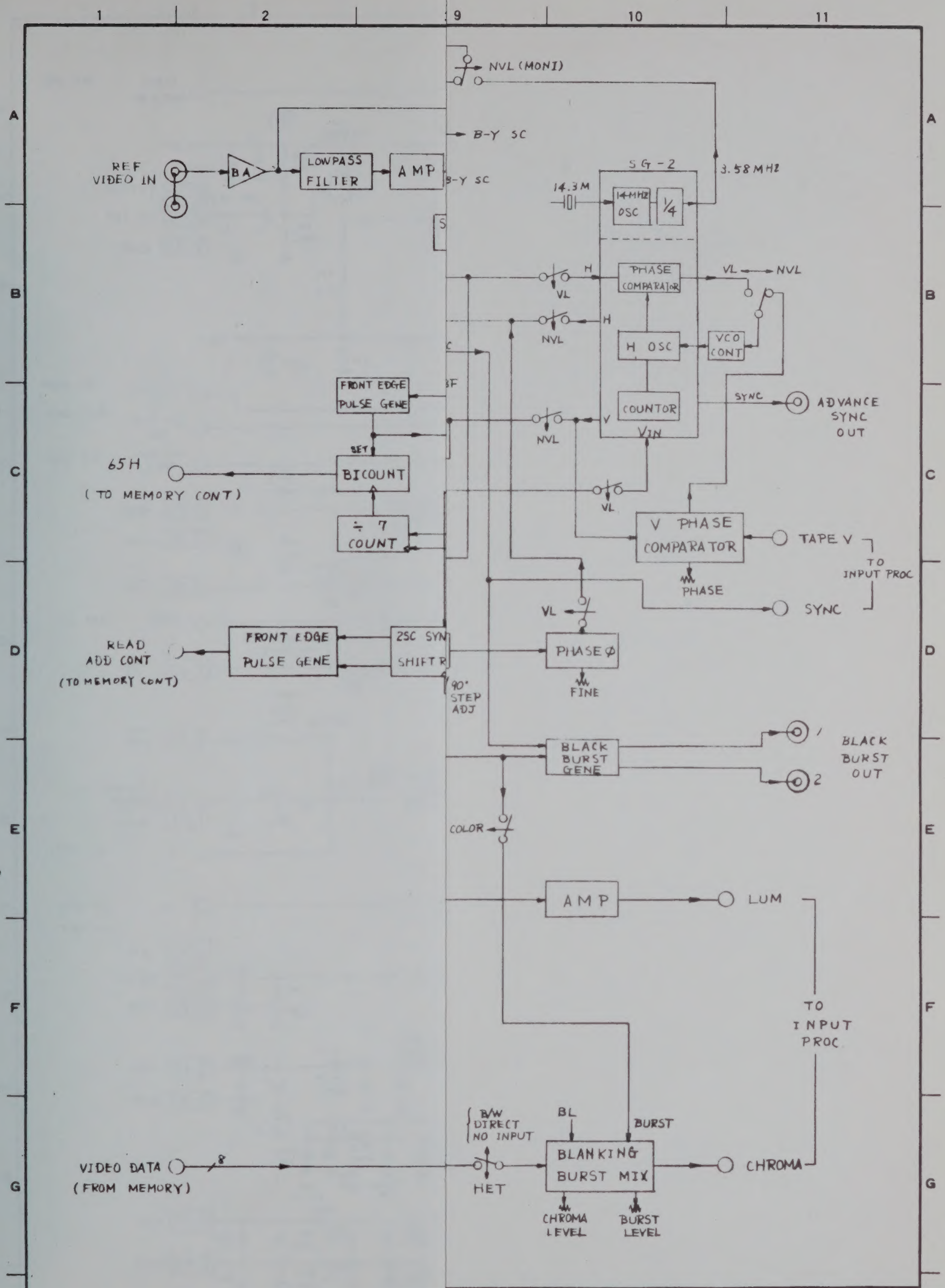
SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
L 1	Inductance	FL 9H 100M	
2	"	"	
3	"	"	
4	"	FL 5H 150K	
5	"	"	
6	"	FL 5H 150K	
T 1	Trance	EP 111-500	
TP 1	Test Pin	LC1-S	
2	"	"	
3	"	"	
4	"	"	
5	"	"	
6	"	"	
7	"	"	
8	"	"	
9	"	"	
10	"	"	
11	"	"	
12	"	"	
13	"	"	
14	"	"	
15	"	"	
J 1	Connector	TC 31-14	
2	"	"	
3	"	"	
4	"	"	
5	"	IL-G 03P S3L2-E	

FA-410N MEMORY BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
J 6	Connector	IL-G 05P-S3L2-E	
7	"	TN 50P-06-L1	
6 A	IC Socket	18 Pin	
B	"	"	
C	"	"	
D	"	"	
E	"	"	
F	"	"	
H	"	"	
K	"	"	
L	"	"	
M	"	"	
N	"	"	
P	"	"	
R	"	"	
S	"	"	
7 A	"	"	
B	"	"	
C	"	"	
D	"	"	
E	"	"	
F	"	"	
H	"	"	
R	"	"	
L	"	"	
M	"	"	
N	"	"	

FA-410N MEMORY BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
7 P	IC Socket	18 Pin	
R	"	"	
S	"	"	
J 1	Housing	Plug for IC 31-14	
2	"	"	
3	"	"	
4	"	"	
5	"	IL-03S-S3L	
6	"	IL-05S-S3L	
7	"	TN-50H-06-A1	
"	Pin	003P-2110	
	TP Terminal for GND	FTR-45-115	

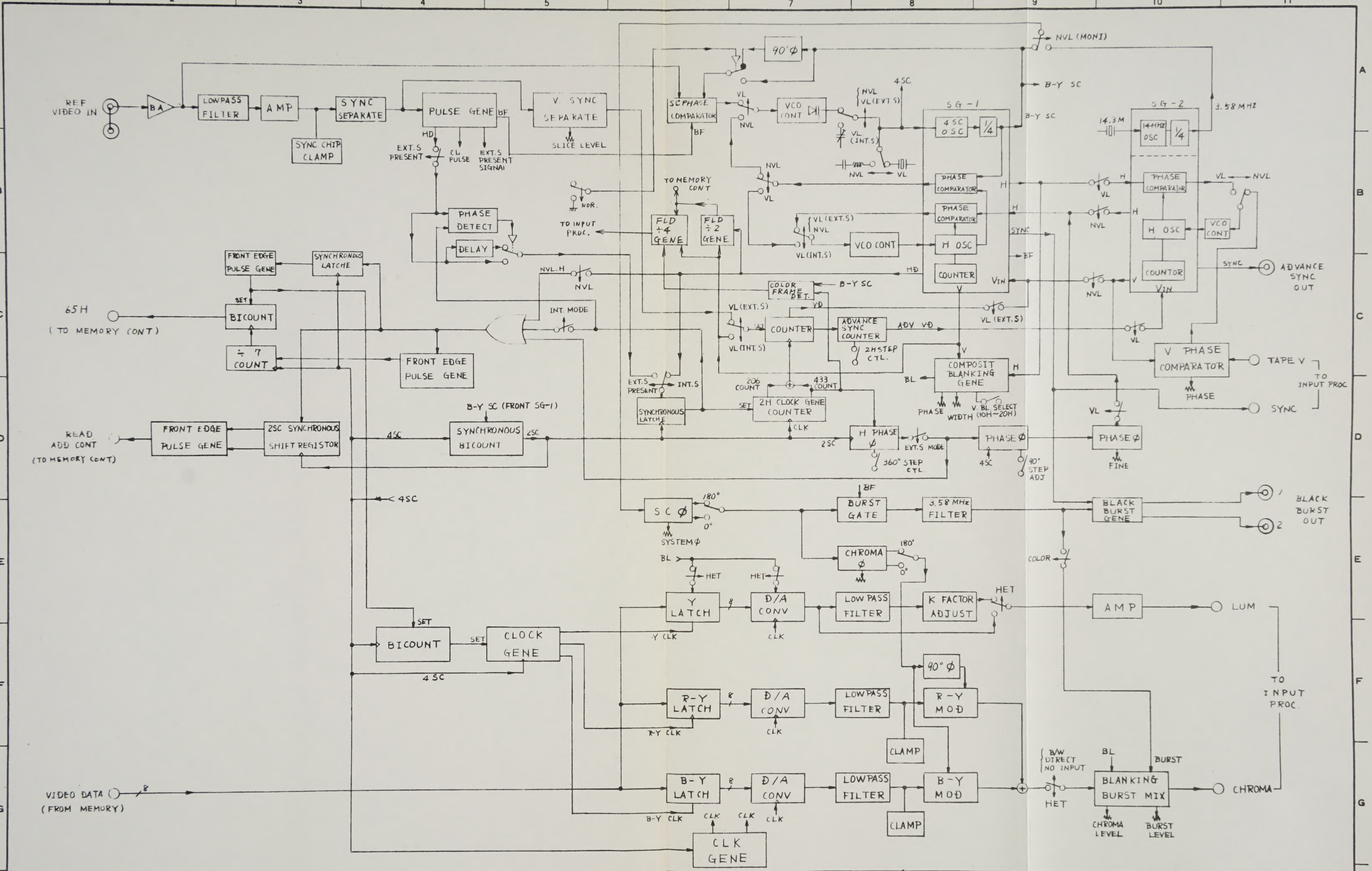

NVL (MONI)
B-Y SC
REF VIDEO IN
BA
LOWPASS FILTER
AMP
B-Y SC
SG-2
3.58MHz
14.3M
14MHz OSC
1/4
H
PHASE COMPARATOR
VL
NVL
VL
H
NVL
H OSC
VCO CONT
C
BF
FRONT EDGE PULSE GENE
COUNTOR
SYNC
ADVANCE SYNC OUT
V
NVL
VIN
SET
65H
(TO MEMORY CONT)
BICOUNT
VL
÷7 COUNT
V PHASE COMPARATOR
TAPE V
TO INPUT PROC
PHASE
SYNC
VL
READ ADD CONT (TO MEMORY CONT)
FRONT EDGE PULSE GENE
2SC SYN SHIFT R
PHASE φ
FINE
90° STEP ADJ
BLACK BURST GENE
1
2
BLACK BURST OUT
COLOR
AMP
LUM
TO INPUT PROC
B/W DIRECT NO INPUT
BL
BURST
VIDEO DATA (FROM MEMORY)
8
HET
BLANKING BURST MIX
CHROMA
CHROMA LEVEL
BURST LEVEL
1
2
9
10
11
A
B
C
D
E
F
G
H

図法	製図	設計	検図	承認	図名
/	山下	AK	宮原		FA410 N OUTPUT PROC. BLOCK DIAGRAM

月日	製番	図番	部番
		A2-3449	

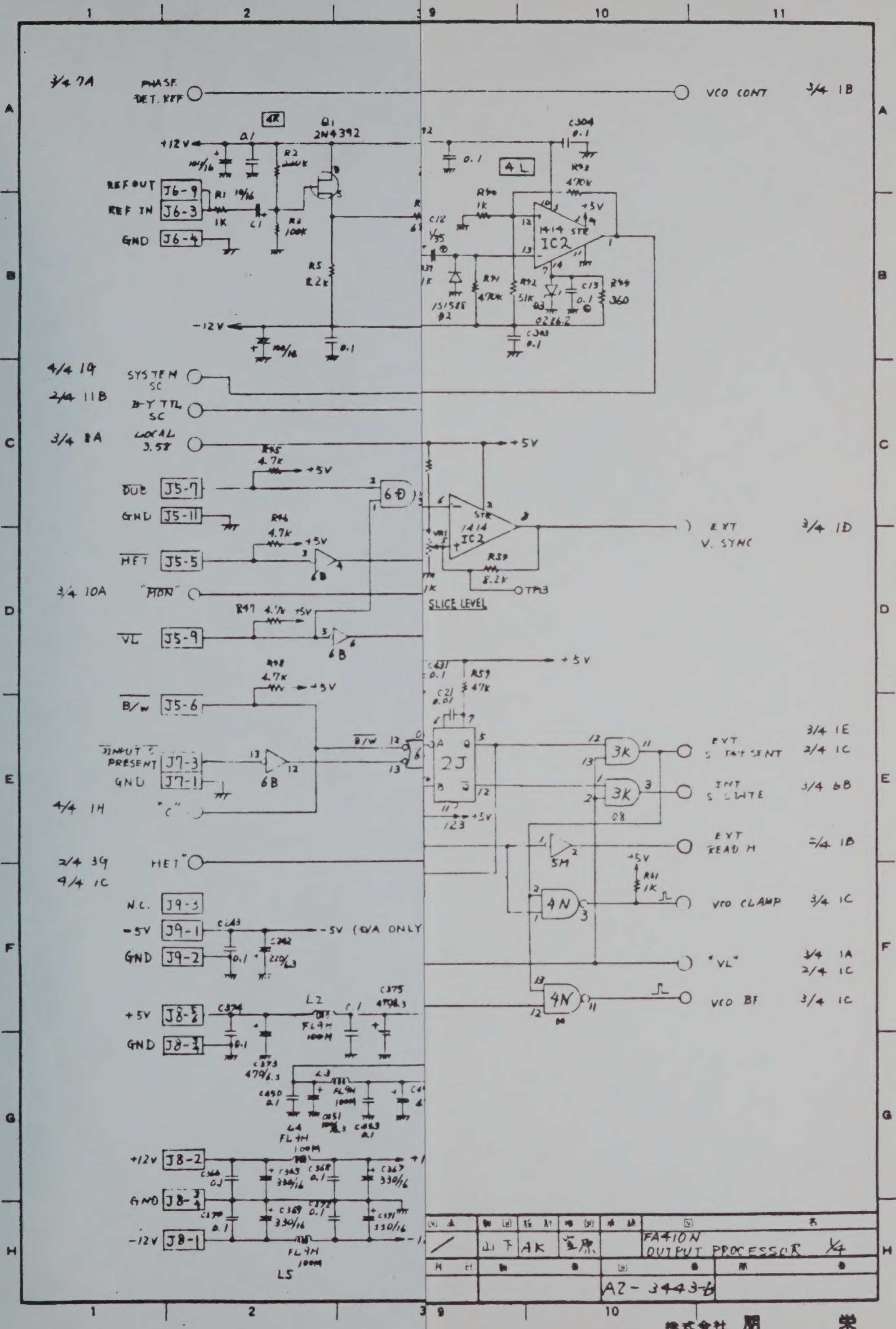
株式会社 朋栄

FOR.A

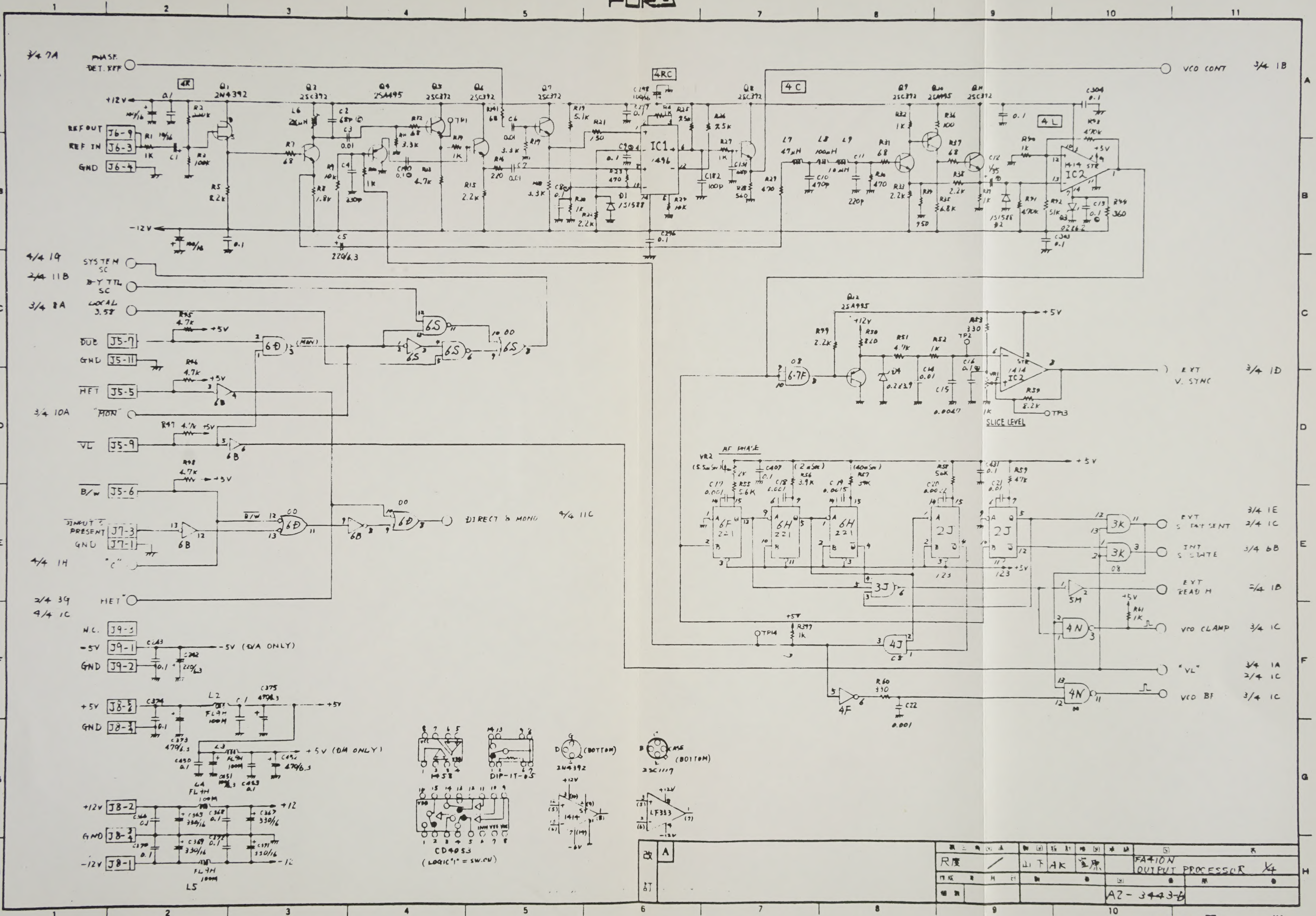

REF VIDEO IN
BA
LOWPASS FILTER
AMP
SYNC CHIP CLAMP
SYNC SEPARATE
PULSE GENE
BF
HD
EXT.S PRESENT
CL PULSE
EXT.S PRESENT SIGNAI
V. SYNC SEPARATE
SLICE LEVEL
NOR.
TO INPUT PROC.
PHASE DETECT
DELAY
NVL.H
NVL
FRONT EDGE PULSE GENE
SYNCHRONOUS LATCHE
SET
BICOUNT
65H
(TO MEMORY CONT)
÷ 7 COUNT
FRONT EDGE PULSE GENE
INT. MODE
READ ADD CONT
(TO MEMORY CONT)
FRONT EDGE PULSE GENE
2SC SYNCHRONOUS SHIFT REGISTOR
4SC
B-Y SC (FRONT SG-1)
SYNCHRONOUS BICOUNT
2SC
< 4SC
90°Φ
NVL (MONI)
B-Y SC
SC PHASE COMPARATOR
BF
VL
NVL
VCO CONT
4SC
NVL
VL (EXT.S)
VL (INT.S)
NVL ↔ VL
SG-1
4SC OSC
1/4
PHASE COMPARATOR
PHASE COMPARATOR
H OSC
COUNTER
VIN
H
SYNC
BF
HD
TO MEMORY CONT
FLD ÷4 GENE
FLD ÷2 GENE
VL (EXT.S)
NVL
VL (INT.S)
VCO CONT
COLOR FRAME DET.
B-Y SC
VD
VL (EXT.S)
SET
COUNTER
VL (INT.S)
ADVANCE SYNC COUNTER
ADV VD
2H STEP CTL.
V
COMPOSIT BLANKING GENE
BL
PHASE
WIDTH
V. BL SELECT (10H~20H)
EXT.S PRESENT
INT.S
SYNCHRONOUS LATCHE
206 COUNT
433 COUNT
2H CLOCK GENE COUNTER
CLK
H PHASE Φ
2SC
EXT.S MODE
360° STEP CTL.
PHASE Φ
4SC
90° STEP ADJ
3.58MHz
SG-2
14.3M
14MHz OSC
1/4
PHASE COMPARATOR
VL ↔ NVL
H OSC
VCO CONT
COUNTOR
V
VIN
SYNC
ADVANCE SYNC OUT
V PHASE COMPARATOR
PHASE
TAPE V
SYNC
TO INPUT PROC
PHASE Φ
FINE
SC Φ
SYSTEM Φ
180°
0°
BURST GATE
3.58 MHz FILTER
BLACK BURST GENE
1
2
BLACK BURST OUT
CHROMA Φ
180°
0°
COLOR
BL
HET
Y LATCH
8
D/A CONV
CLK
LOW PASS FILTER
K FACTOR ADJUST
AMP
LUM
TO INPUT PROC.
SET
BICOUNT
SET
CLOCK GENE
Y CLK
4SC
90°Φ
R-Y LATCH
R-Y CLK
D/A CONV
LOW PASS FILTER
R-Y MOD
CLAMP
VIDEO DATA
(FROM MEMORY)
B-Y LATCH
B-Y CLK
D/A CONV
LOWPASS FILTER
B-Y MOD
CLAMP
B/W DIRECT NO INPUT
BL
BURST
BLANKING BURST MIX
CHROMA
CHROMA LEVEL
BURST LEVEL
CLK GENE

改訂	A	第三角図法	製図	設計	検図	承認	図名
		尺度 ／	山下	AK	多原		FA410 N OUTPUT PROC. BLOCK DIAGRAM
		作成 年 月 日	製番		図番		部番
		個数			A2-3449		

株式会社 朋栄


3/4 7A
PHASE DET. REF
VCO CONT
3/4 1B
Q1 2N4392
4R
+12V
A1
4L
C304 0.1
R43 470k
R40 1K
+5V
1414 STR
IC2
REF OUT J6-9
REF IN J6-3
GND J6-4
R1 1K
C1
R2 100k
R3 100k
R5 R2k
C12 1/35
15158E D2
R41 470k
R42 51K
D3 0286.2
C13 0.1
R44 360
-12V
100/16
0.1
C303 0.1
4/4 1G SYSTEM SC
2/4 11B B-Y TTL SC
3/4 8A LOCAL 3.58
+5V
R45 4.7k
DUE J5-7
GND J5-11
6D
1414 IC2
R46 4.7k
HET J5-5
6B
EXT V. SYNC
3/4 1D
R39 8.2k
TP3
1K
SLICE LEVEL
3/4 10A "MON"
R47 4.7k
VL J5-9
6B
C431 0.1
R59 47k
C21 0.01
R48 4.7k
B/W J5-6
B/W
INPUT S PRESENT J7-3
GND J7-1
6B
2J
123
3K
08
EXT S PRESENT
3/4 1E
2/4 1C
INT S SWITE
3/4 6B
4/4 1H "C"
2/4 3G
4/4 1C
HET
5M
EXT READ H
2/4 1B
R61 1K
4N
VCO CLAMP
3/4 1C
N.C. J9-3
-5V J9-1
GND J9-2
C243
C242 220/6.3
-5V (D/A ONLY
"VL"
3/4 1A
2/4 1C
VCO BF
3/4 1C
+5V J8-5/6
GND J8-3/4
C374
L2 FL4H 100M
C375 470/6.3
C373 470/6.3
L3 FL4H 100M
C450 0.1
C451 100/6.3
C453 0.1
L4 FL4H 100M
+12V J8-2
GND J8-3/4
-12V J8-1
C366 0.1
C365 330/16
C368 0.1
C367 330/16
C370 0.1
C369 330/16
C372 0.1
C371 330/16
FL4H 100M
L5
山下
AK
宝原
FA410N OUTPUT PROCESSOR 1/4
AZ-3443-B
株式会社 朋栄
1 2 3 9 10 11
A B C D E F G H

FOR-A


PHASE DET. REF
3/4 7A
VCO CONT
3/4 1B
+12V
-12V
REF OUT J6-9
REF IN J6-3
GND J6-4
Q1 2N4392
Q2 2SC372
Q4 2SA495
Q5 2SC372
Q6 2SC372
Q7 2SC372
Q8 2SC372
Q9 2SC372
Q10 2SA495
Q11 2SC372
4R
4RC
4C
4L
IC1 1496
IC2 1414
L6 22μH
L7 47μH
L8 100μH
L9 10μH
D1 1S1588
D2 1S1588
D3 05Z6.2
C5 220/6.3
SYSTEM SC
4/4 1G
2/4 11B
B-Y TTL SC
LOCAL 3.58
3/4 8A
DUE J5-7
GND J5-11
HET J5-5
"MON"
3/4 10A
VL J5-9
B/W J5-6
INPUT PRESENT J7-3
GND J7-1
"C"
4/4 1H
HET
2/4 3G
4/4 1C
6S
6D
6B
(MON)
DIRECT & MONO
4/4 11C
N.C. J9-3
-5V J9-1
GND J9-2
-5V (DVA ONLY)
+5V J8-5/6
GND J8-3/4
L2 FL9H 100M
+5V (DM ONLY)
+12V J8-2
GND J8-3/4
-12V J8-1
L5 FL9H 100M
Q12 2SA495
6·7F
1414 IC2
SLICE LEVEL
TP2
TP3
EXT V. SYNC
3/4 1D
VR2 AF PHASE
6F 221
6H 221
2J 123
3K
3J
4J
4N
5M
4F
TP14
EXT S PRESENT
3/4 1E
2/4 1C
INT S STATE
3/4 6B
EXT READ H
2/4 1B
VCO CLAMP
3/4 1C
"VL"
3/4 1A
2/4 1C
VCO BF
3/4 1C
14S8
DIP-1T-05
2N4392 (BOTTOM)
2SC1117 (BOTTOM)
CASE
CD4053
(LOGIC "1" = SW.ON)
1414
LF353
改
A
訂

尺度 /
山下 AK 峯原
FA410N
OUTPUT PROCESSOR 1/4
A2-3443-B

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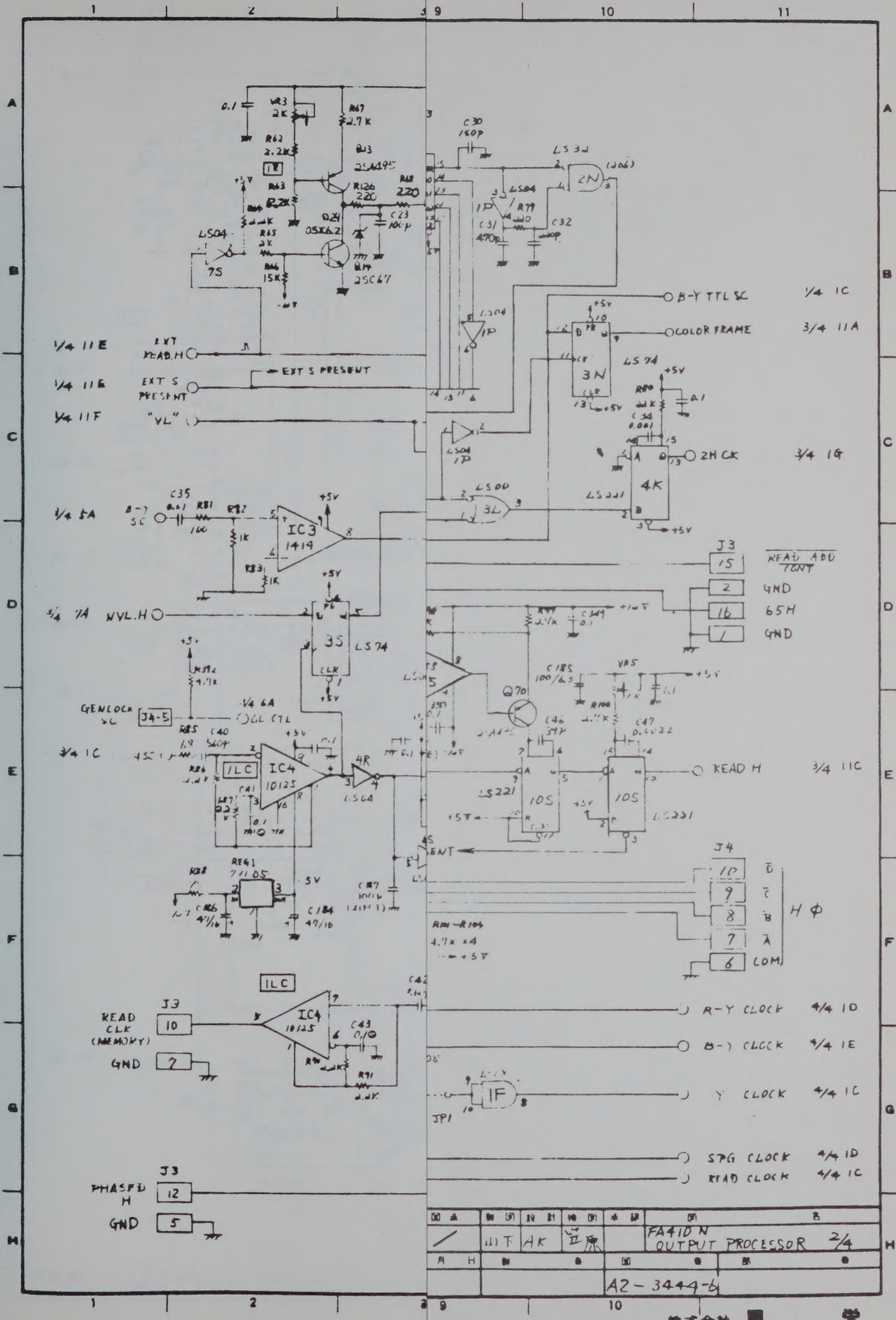
1/4 11E EXT READ.H
1/4 11E EXT S PRESENT
EXT S PRESENT
1/4 11F "VL"
3/4 5A B-Y SC
C35 0.01
R81 100
R82 1k
IC3 1414
R83 1k
+5V
3/4 7A NVL.H
3S LS74
GENLOCK SC
J4-5
1/4 6A GL CTL
R394 4.7k
3/4 1C +SC
R85 6.8
C40 560P
R86 2.2k
IC4 10125
1LC
4R LS04
REG1 7805
C184 47/10
C86 47/16
READ CLK (MEMORY)
J3 10
GND 2
IC4 10125
C43 0.1
R91 2.2k
C42
PHASED H
J3 12
GND 5
VR3 2K
R67 2.7K
R62 2.2K
Q13 2SA495
R63 2.2K
R65 2K
R66 15K
Q24 2SC67
R126 220
R68 220
C23 100p
LS04 7S
C30 150p
LS32 2N
1P LS04
R79 220
C31 470p
C32
B-Y TTL SC 1/4 1C
COLOR FRAME 3/4 11A
LS74 3N
R80 22K
C34 0.001
2H CK 3/4 1G
LS221 4K
LS00 3L
LS04 1P
J3
15 READ ADD CONT
2 GND
16 65H
1 GND
C349 0.1
Q70
C185 100/6.3
VR5
C46 33P
C47 0.0022
READ H 3/4 11C
LS221 10S
LS221 10S
C87 100/16
J4
10 D
9 C
8 B
7 A
6 COM
H Φ
R101-R104 4.7k ×4 +5V
R-Y CLOCK 4/4 1D
B-Y CLOCK 4/4 1E
1F
JP1
Y CLOCK 4/4 1C
SPG CLOCK 4/4 1D
READ CLOCK 4/4 1C

山下 AK 笠原

FA410 N OUTPUT PROCESSOR 2/4

A2-3444-6

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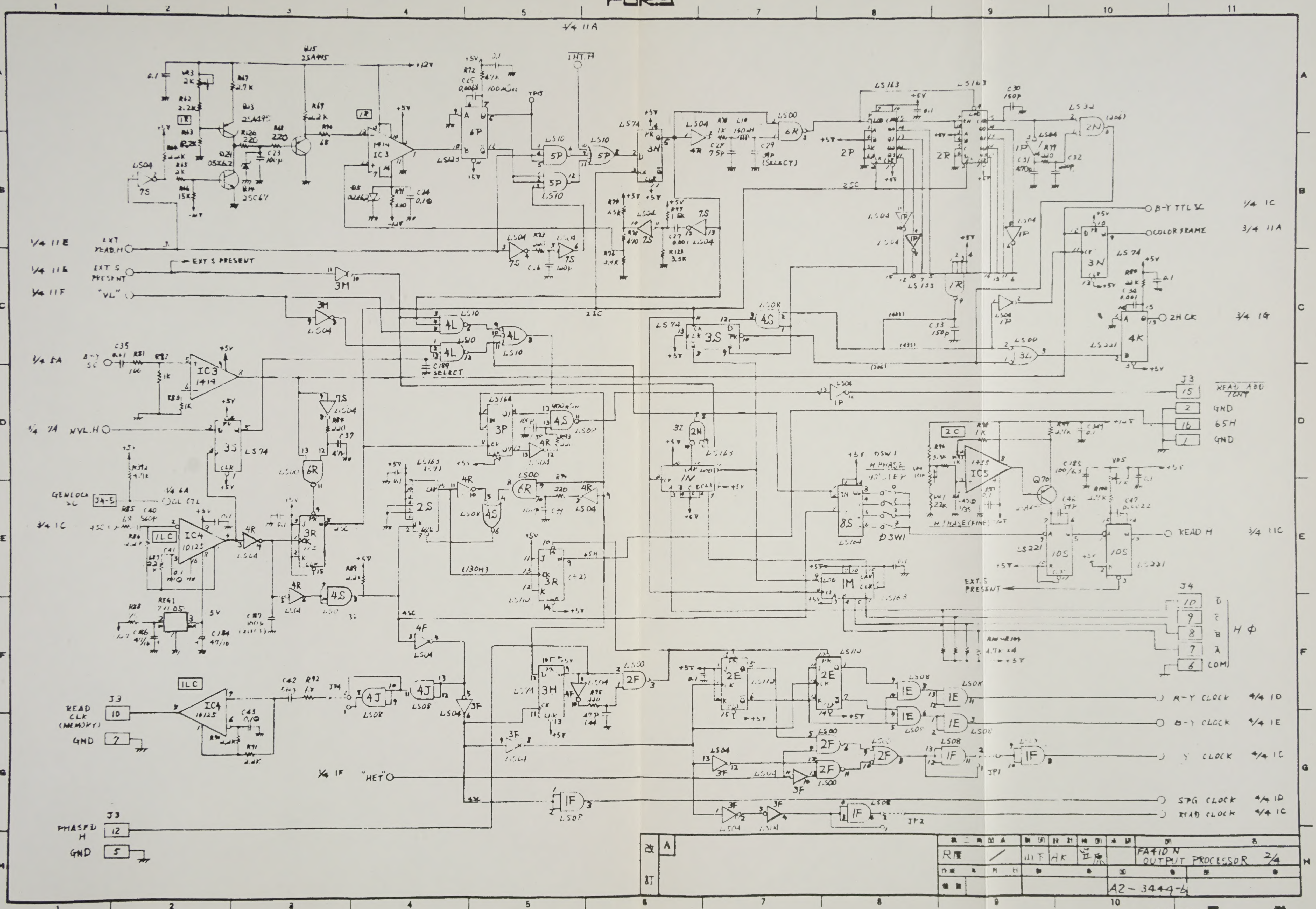
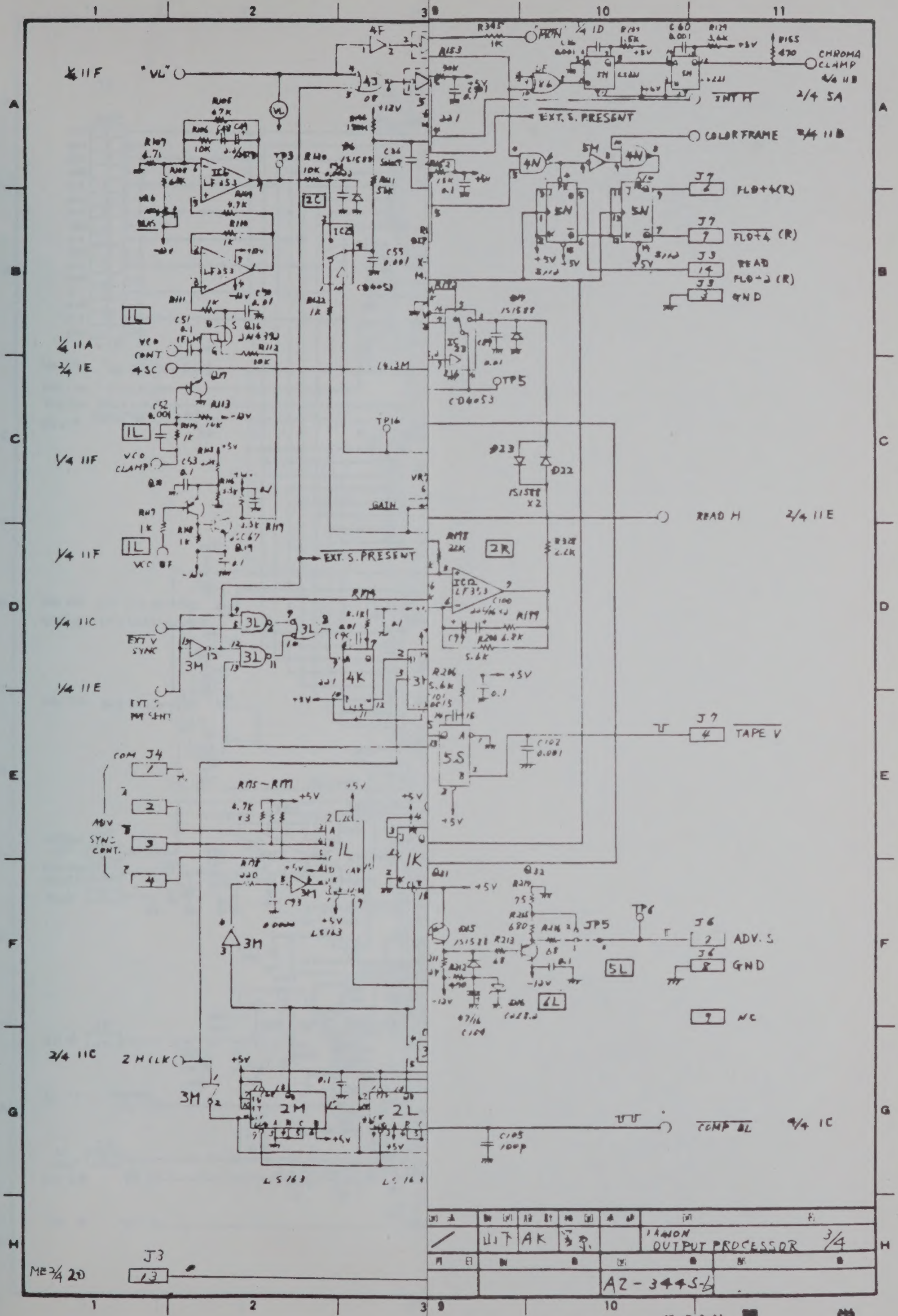

1/4 11A
INT.H
+12V
IC3
1414
6P
5P
LS10
LS74
3H
LS04
6R
LS00
LS163
2P
2R
LS32
2N
1P
LS133
1R
B-Y TTL SC 1/4 1C
COLOR FRAME 3/4 11A
3N
LS74
4K
LS221
2H CK 3/4 1G
1/4 11E EXT READ.H
1/4 11E EXT S PRESENT
EXT S PRESENT
1/4 11F "VL"
3M
4L
3S
4S
LS08
3L
1/4 5A B-Y SC
C189 SELECT
3/4 7A NVL.H
LS164
3P
4S
J3
15 READ ADD TEST
2 GND
16 65H
1 GND
2N
LS163
1N
DSW1
H PHASE
8S
2C
IC5
Q70
10S
LS221
READ H 3/4 11C
GENLOCK SC
J4-5
1/4 1C
IC4 10125
4R
3R
2S
6R
4S
3R
(÷2)
(130H)
65H
1M
EXT S PRESENT
J4
10 D
9 C
8 B
7 A
6 COM
H Φ
REG1 78L05
4F
2E
1E
R-Y CLOCK 4/4 1D
B-Y CLOCK 4/4 1E
2F
1F
JP1
Y CLOCK 4/4 1C
READ CLK (MEMORY)
J3
10
7 GND
4J
3F
1/4 1F "HET"
SPG CLOCK 4/4 1D
READ CLOCK 4/4 1C
JP2
PHASED H
J3
12
5 GND
改 A
訂
尺度
山下
AK
FA410N
OUTPUT PROCESSOR 2/4
A2-3444-6

株式会社 朋栄


"VL"
1/4 11F
1/4 11A
2/4 1E
VCO CONT
4SC
1/4 11F
VCO CLAMP
1/4 11F
VCO BF
1/4 11C
EXT V SYNC
1/4 11E
EXT S PRESENT
COM J4
ADV SYNC CONT.
RMS~RM
2/4 11C
2 H CLK
3M
2M
2L
LS163
LF353
IC12
CD4053
CD4053
14.3M
TP3
TP5
TP16
TP6
GAIN
VR7
EXT. S. PRESENT
EXT. S. PRESENT
R345
1K
MON
1/4 1D
CHROMA CLAMP
4/4 11B
2/4 5A
INT H
COLORFRAME
2/4 11B
4N
5M
5N
J7
FLD÷4(R)
FLD÷4 (R)
J3
READ FLD÷2 (R)
GND
D23
D22
1S1588 x2
READ H
2/4 11E
LF353
2R
3L
4K
5S
1K
1L
3M
J7
TAPE V
JP5
5L
6L
J6
ADV. S
GND
NC
COMP BL
4/4 1C
J3
13
ME 2/4 20
1L
2C
IAMON
OUTPUT PROCESSOR
3/4
山下
AK
A2-3445-6
1
2
3
9
10
11
A
B
C
D
E
F
G
H

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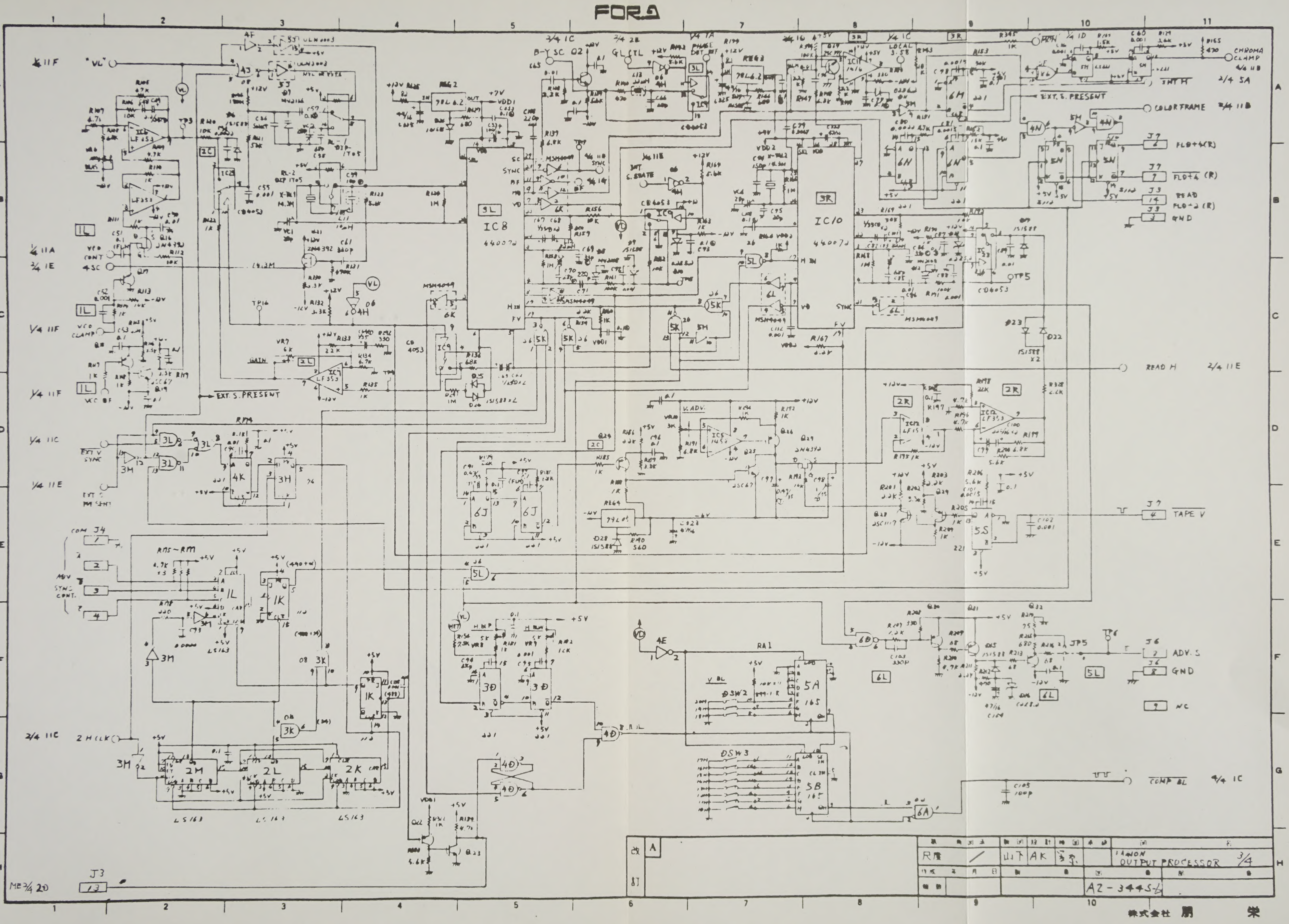
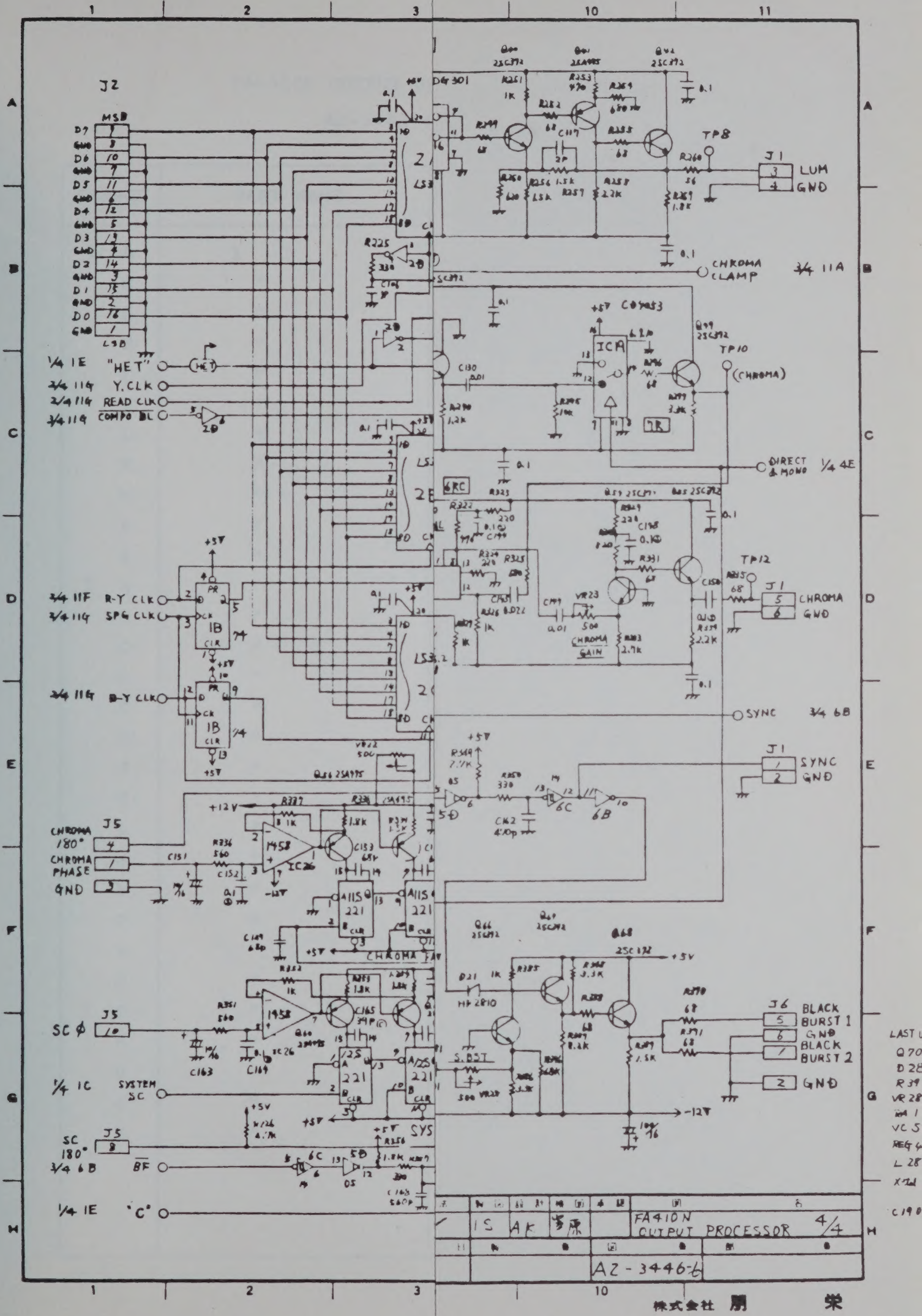
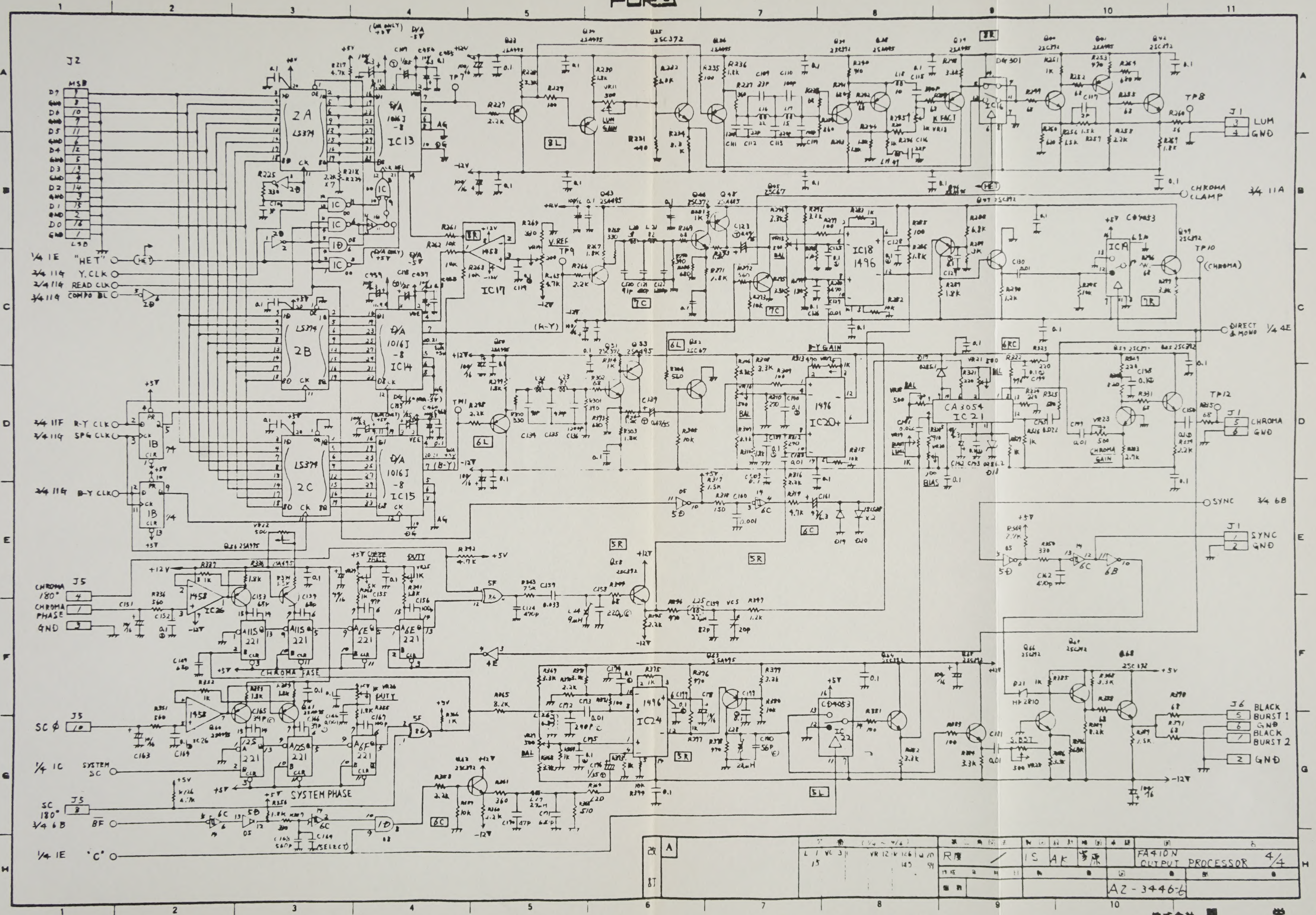

FOR.A
"VL"
4/11F
1/11A
3/4 1E
VCO CONT
4SC
VCO CLAMP
VCC BF
1/4 11F
1/4 11C
1/4 11E
EXT V SYNC
EXT S PRESENT
EXT. S. PRESENT
COM J4
ADV SYNC CONT.
2/4 11C
2 H CLK
J3
13
ME 3/4 20
ULN 2003
LF353
IC8
44007
IC10
44007
78L62
VDD1
VDD2
3/4 1C
B-Y SC Q2
3/4 2E
GL CTL
PHASE DET REF
3/4 11B
4/4 1C
LOCAL 3.58
CHROMA CLAMP
4/4 1B
2/4 5A
INT H
COLORFRAME
3/4 11B
FLD+4(R)
FLD+4 (R)
FLD÷2 (R)
READ
GND
J7
J3
READ H
2/4 11E
TAPE V
ADV. S
GND
NC
J6
JP5
TP5
TP6
COMP BL
4/4 1C
DSW2
DSW3
RA1
V.BL
V.ADV
GAIN
CD4053
MSM4049
14.3M
LS163
165
改
訂
A
尺度
山下
AK
IAMON
OUTPUT PROCESSOR
3/4
作成 年 月 日
A2-3445-6
株式会社 朋栄


J2
MSB
D7 GND D6 GND D5 GND D4 GND D3 GND D2 GND D1 GND D0 GND
LSB
1/4 1E "HET"
2/4 11G Y.CLK
2/4 11G READ CLK
3/4 11G COMPO BL
3/4 11F R-Y CLK
2/4 11G SPG CLK
3/4 11G B-Y CLK
CHROMA 180°
CHROMA PHASE
GND
J5
SC Φ
1/4 1C SYSTEM SC
SC 180° 3/4 6B
BF
1/4 1E 'C'
DG301
Q40 2SC372
Q41 2SA495
Q42 2SC372
TP8
J1
LUM
GND
CHROMA CLAMP 3/4 11A
+5V CD4053
ICA
Q44 2SC372
TP10
(CHROMA)
DIRECT & MONO 1/4 4E
Q57 2SC371
Q65 2SC372
TP12
CHROMA
GND
VR23 500 CHROMA GAIN
SYNC 3/4 6B
SYNC
GND
Q56 2SA495
1458
IC26
A115 221
CHROMA
HF2810
S.BST
BLACK BURST 1
GND
BLACK BURST 2
GND
J6
-12V
+5V
+12V
LAST U
Q70
D28
R39
VR28
VC5
REG
L28
C19

FA410N
OUTPUT PROCESSOR 4/4
AZ-3446-6

株式会社 朋 栄

FOR-A


J2
MSB
LSB
D7
D6
D5
D4
D3
D2
D1
D0
GND
2A LS374
2B LS374
2C LS374
D/A 1016J-8 IC13
D/A 1016J-8 IC14
D/A 1016J-8 IC15
IC17 1458
IC18 1496
IC20 1496
CA3054 IC21
IC24 1496
IC16
IC22 CD4053
IC26 1458
1/4 1E "HET"
3/4 11G Y.CLK
3/4 11G READ CLK
3/4 11G COMPO BL
3/4 11F R-Y CLK
3/4 11G SPG CLK
3/4 11G B-Y CLK
V.REF
TP7
TP8
TP9
TP10 (CHROMA)
TP11
TP12
LUM GAIN
K FACT
(R-Y)
(B-Y)
B-Y GAIN
BAL
BIAS
CHROMA GAIN
CHROMA CLAMP 3/4 11A
DIRECT & MONO 1/4 4E
SYNC 3/4 6B
J1
LUM
GND
CHROMA
SYNC
J5
CHROMA 180°
CHROMA PHASE
GND
CHROMA FASE
CHROMA FINE
DUTY
SC ϕ
SYSTEM PHASE
1/4 1C SYSTEM SC
SC 180°
3/4 6B BF
1/4 1E 'C'
(SELECT)
S.BST
J6
BLACK BURST 1
BLACK BURST 2
GND
8L
7C
6L
6RC
7R
5R
5L
6C
+5V
+12V
-12V
1 2 3 4 5 6 7 8 9 10 11
A B C D E F G H
改訂
A
尺度
FA410N
OUTPUT PROCESSOR 4/4
AZ-3446-6

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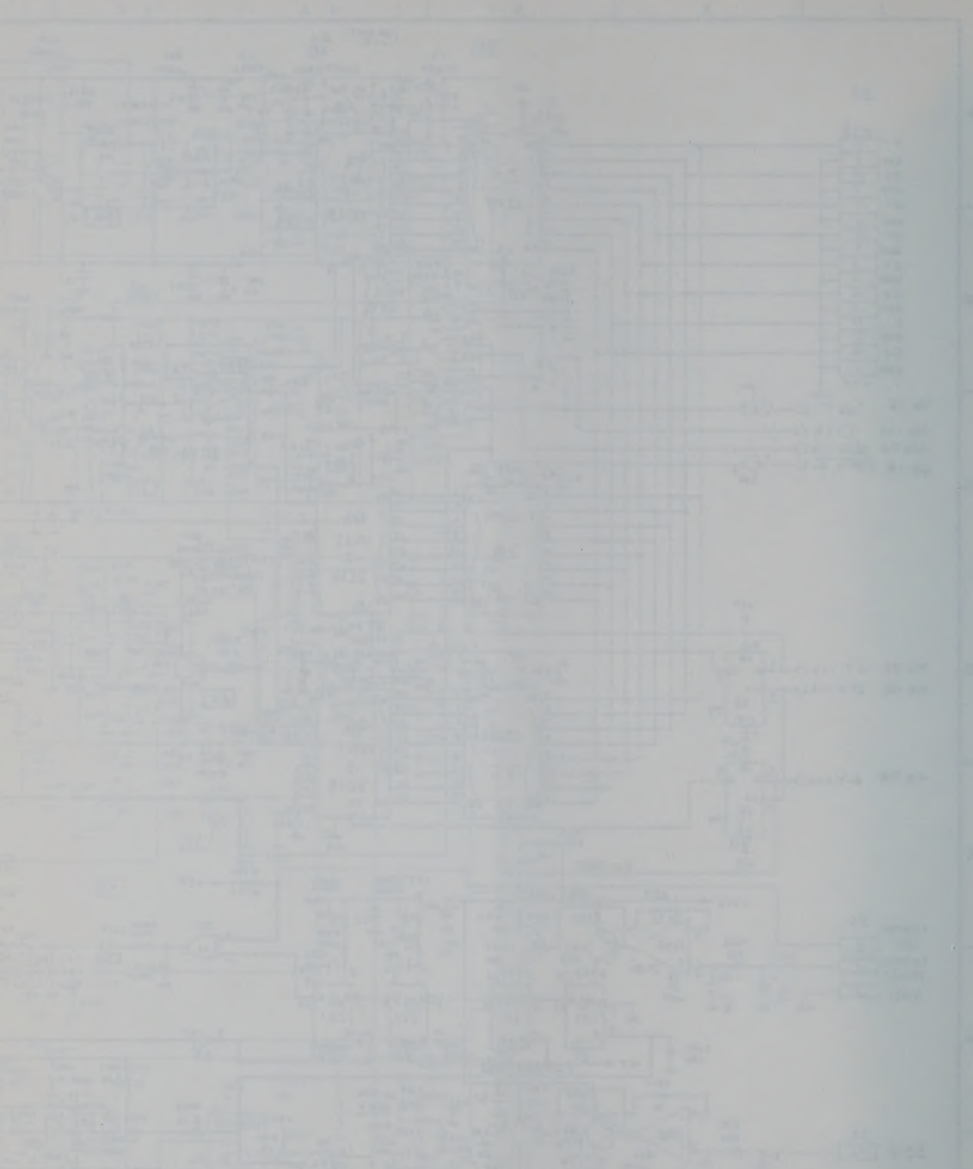


FA-410N OUTPUT PROCESSOR BOARD

A2-3443-4~3446-4

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
1 B	I C	SN 74 LS 74	
C	"	00	
D	"	08	
E	"	"	
F	"	"	
K	"	112	
L	"	163	
M	"	"	
N	"	"	
P	"	04	
R	"	133	
2 A	"	374	
B	"	"	
C	"	"	
D	"	04	
E	"	112	
F	"	00	
J	"	123	
K	"	163	
L	"	"	
M	"	"	
N	"	32	
P	"	163	
R	"	"	
S	"	"	
3 D	"	221	
F	"	04	
H	"	74	
J	"	10	
K	"	08	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
3 L	I C	SN 74 LS 00	
M	"	" " 04	
N	"	" " 74	
P	"	" " 164	
R	"	" " 112	
S	"	" " 74	
4 D	"	" " 00	
E	"	" " 04	
F	"	" " "	
H	"	SN 7406	
J	"	SN 74 LS 08	
K	"	" " 221	
L	"	" " 10	
N	"	" " 00	
R	"	" " 04	
S	"	" " 08	
5 A	"	" " 165	
B	"	" " "	
D	"	" " 05	
F	"	" " 86	
H	"	" " 221	
J	"	ULN 2003	
K	"	SN 74 LS 26	
L	"	" " "	
M	"	" " 04	
N	"	SN 74 S 112	
"	IC Socket	14 Pin	
P	I C	SN 74 LS 10	
S	"	" " 221	
6 A	"	" " 02	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
6 B	I C	SN 74 LS 04	
C	"	14	
D	"	00	
E	"	221	
F	"	"	
H	"	"	
J	"	"	
K	"	MSM 4049	
L	"	"	
M	"	SN 74 LS 221	
N	"	" " "	
P	"	" " 123	
R	"	" " 00	
S	"	" " "	
6,7 F	"	" " 08	
7 S	"	" " 04	
8 S	"	" " 164	
10 S	"	" " 221	
11 S	"	" " "	
12 S	"	" " "	
IC 1	"	MC 1496 L	
"	IC Socket	14 Pin	
IC 2	I C	MC 1414 P	
"	IC Socket	14 Pin	
IC 3	I C	MC 1414 P	
"	IC Socket	14 Pin	
IC 4	I C	HD 10125	
"	IC Socket	16 Pin	
IC 5	I C	MC 1458 CP	
"	IC Socket	8 Pin	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
IC 6	I C	LF 353 N	
"	IC Socket	8 Pin	
IC 7	I C	LF 353 N	
"	IC Socket	8 Pin	
IC 8	I C	HD 440072	
"	IC Socket	28 Pin	
IC 9	I C	CD 4053 BE	
"	IC Socket	16 Pin	
IC 10	I C	HD 440072	
"	IC Socket	28 Pin	
IC 11	I C	MC 1414 P	
"	IC Socket	14 Pin	
IC 12	I C	LF 353 N	
"	IC Socket	8 Pin	
IC 13	I C	TCD 1016 J	
"	IC Socket	40 Pin	
IC 14	I C	TDC 1016 J	
"	IC Socket	40 Pin	
IC 15	I C	TDC 1016 J	
"	IC Socket	40 Pin	
IC 16	I C	DG 301 CJ	
"	IC Socket	14 Pin	
IC 17	I C	MC 1458 CP	
"	IC Socket	8 Pin	
IC 18	I C	MC 1496 L	
"	IC Socket	14 Pin	
IC 19	I C	CD 4053 BE	
"	IC Socket	16 Pin	
IC 20	I C	MC 1496 L	
"	IC Socket	14 Pin	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
IC 21	I C	CA 3054	
"	IC Socket	14 Pin	
IC 22	I C	CD 4053 BE	
"	IC Socket	16 Pin	
IC 23	I C	CD 4053 BE	
"	IC Socket	16 Pin	
IC 24	I C	MC 1496	
"	IC Socket	14 Pin	
IC 25	I C	CD 4053 BE	
"	IC Socket	16 Pin	
IC 26	I C	MC 1458 CP	
"	IC Socket	8 Pin	
Q 1	Transistor	2N 4392	
2	"	2 SC 372	
3	"	2 SC 372	
4	"	2 SA 495	
5	"	2 SC 372	
6	"	"	
7	"	"	
8	"	"	
9	"	"	
10	"	2 SA 495	
11	"	2 SC 372	
12	"	2 SA 495	
13	"	"	
14	"	2 SC 67	
15	"	2 SA 495	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
Q 16	Transistor	2 N 4392	
17	"	2 SC 372	
18	"	2 SA 495	
19	"	2 SC 67	
20	"	Deleted	
21	"	2 N 4392	
22	"	2 SA 495	
23	"	2 SC 372	
24	"	2 SA 495	
25	"	2 SC 67	
26	"	2 SA 495	
27	"	2 N 4392	
28	"	2 SC1117	
29	"	2 SA 495	
30	"	"	
31	"	"	
32	"	"	
33	"	2 SA 495	
34	"	"	
35	"	2 SC 372	
36	"	2 SC 495	
37	"	2 SC 372	
38	"	2 SA 495	
39	"	2 SA 495	
40	"	2 SC 372	
41	"	2 SA 495	
42	"	2 SC 372	
43	"	2 SA 495	
44	"	2 SC 372	
45	"	2 SC 67	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
Q 46	Transistor	2 SA 495	
47	"	2 SC 372	
48	"	2 SA 495	
49	"	2 SC 372	
50	"	2 SA 495	
51	"	2 SC 372	
52	"	2 SC 67	
53	"	2 SA 495	
54	"	2 SC 372	
55	"	"	
56	"	2 SA 495	
57	"	"	
58	"	2 SC 372	
59	"	Deleted	
60	"	2 SA 495	
61	"	"	
62	"	2 SC 372	
63	"	2 SA 495	
64	"	2 SC 372	
65	"	"	
66	"	"	
67	"	"	
68	"	"	
69	"	"	
70	"	2 SA 495	

FA-410N INPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
D 1	Diode	IS 1588	
2	"	"	
3	"	02Z 6.2	
4	"	02Z 3.9	
5	"	02Z 6.2	
6	"	IS 1588	
7	"	MV 2114	
8	"	MV 2108	
9	"	IS 1588	
10	"	02Z 5.1	
11	"	02Z 6.2	
12	"	MV 2108	
13	"	02Z 5.1	
14	"	IS 1588	
15	"	"	
16	"	02Z 8.2	
17	"	02Z 5.1	
18	"	02Z 6.2	
19	"	IS 1588	
20	"	"	
21	"	HP 2810	
22	"	IS 1588	
23	"	"	
24	"	"	
25	"	"	
26	"	"	
27	"	"	
28	"	"	
29	"	05Z 6.2	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS		REMARKS
R 1	Fixed Resistor	CR 25JU	102	
2	"	"	224	
3	"	"	104	
4	"	"	102	
5	"	"	822	
6	"	"	562	
7	"	"	680	
8	"	"	182	
9	"	"	103	
10	"	"	102	
11	"	"	332	
12	"	"	680	
13	"	"	472	
14	"	"	102	
15	"	"	222	
16	"	"	221	
17	"	"	332	
18	"	"	332	
19	"	"	512	
20	"	"	102	
21	"	"	151	
22	"	"	222	
23	"	"	471	
24	"	"	103	
25	"	"	752	
26	"	"	"	
27	"	"	102	
28	"	"	561	
29	"	"	471	
30	"	"	"	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
R 31	Fixed Resistor	CR 25JU 680	
32	"	" 102	
33	"	" 222	
34	"	" 751	
35	"	" 682	
36	"	" 101	
37	"	" 680	
38	"	" 222	
39	"	" 102	
40	"	" "	
41	"	" 474	
42	"	" 513	
43	"	" 474	
44	"	" 361	
45	"	" 472	
46	"	" "	
47	"	" "	
48	"	" "	
49	"	" 222	
50	"	" 821	
51	"	" 472	
52	"	" 102	
53	"	" 331	
54	"	" 822	
55	"	" 562	
56	"	" 392	
57		" 393	
58	"	" 563	
59	"	" 473	
60	"	" 331	

FA-410N OUTPUT PTOCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS		REMARKS
R 61	Fixed Resistor	CR 25JU	102	
62	"	"	222	
63	"	"	222	
64	"	"	222	
65	"	"	202	
66	"	"	153	
67	"	"	272	
68	"	"	221	
69	"	"	222	
70	"	"	680	
71	"	"	331	
72	"	"	473	
73	"	"	221	
74	"	"	152	
75	"	"	471	
76	"	"	392	
77	"	"	152	
78	"	"	102	
79	"	"	221	
80	"	"	223	
81	"	"	101	
82	"	"	102	
83	"	"	"	
84	"	"	221	
85	"	"	680	
86	"	"	222	
87	"	"	"	
88	"	"	750	
89	"	"	222	
90	"	"	"	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
R 91	Fixed Resistor	CR 25JU 222	
92	"	" 680	
93	"	" 221	
94	"	" "	
95	"	" "	
96	"	" 332	
97	"	" 222	
98	"	" 102	
99	"	" 272	
100	"	" "	
101	"	" 472	
102	"	" "	
103	"	" "	
104	"	" "	
105	"	" 473	
106	"	" 103	
107	"	" 472	
108	"	" 683	
109	"	" 472	
110	"	" 102	
111	"	" "	
112	"	" 103	
113	"	" "	
114	"	" 102	
115	"	" 222	
116	"	" 332	
117	"	" 102	
118	"	" "	
119	"	" 332	
120	"	" 103	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS		REMARKS
R 121	Fixed Resistor	CR 25JU	563	
122	"	"	102	
123	"	"	562	
124	"	"	105	
125	"	"	820	
126	"	"	680	
127	"	CR 25JU	681	
128	"	"	332	
129	"	"	362	
130	"	"	332	
131	"	"	474	
132	"	"	332	
133	"	"	223	
134	"	"	472	
135	"	"	102	
136	"	"	683	
137	"	"	682	
138	"	"	222	
139	"	"	562	
140	"	"	471	
141	"	"	680	
142	"	"	562	
143	"	"	103	
144	"	"	820	
145	"	Deleted		
146	"	CR 25JU	681	
147	"	"	222	
148	"	"	682	
149	"	"	222	
150	"	"	331	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS		REMARKS
R 151	Fixed Reisstor	CR 25JU	473	
152	"	"	153	
153	"	"	303	
154	"	"	752	
155		CR 25JU	471	
156	"	"	103	
157	"	"	303	
158	"	"	105	
159	"	"	222	
160	"	"	102	
161	"	"	104	
162	"	"	103	
163	"	"	102	
164	"	"	562	
165	"	"	105	
166	"	"	102	
167	"	"	222	
168	"	"	105	
169	"	"	303	
170	"	"	102	
171	"	"	104	
172	"	"	103	
173	"	"	102	
174	"	"	512	
175	"	"	472	
176	"	"	"	
177	"	"	"	
178	"	"	221	
179	"	"	223	
180	"	"	683	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
R 181	Fixed Resistor	CR 25JU 102	
182	"	" 123	
183	"	" 562	
184	"	" 472	
185	"	" 102	
186	"	" 222	
187	"	" 332	
188	"	" 102	
189	"	" 750	
190	"	" 561	
191	"	" 682	
192	"	" 102	
193	"	" 103	
194	"	" 154	
195	"	" 102	
196	"	" 472	
197	"	" "	
198	"	" 223	
199	"	" 682	
200	"	" 562	
201	"	" 222	
202	"	" 332	
203	"	" 222	
204	"	" 102	
205	"	" "	
206	"	" 562	
207	"	" 122	
208	"	" 331	
209	"	" 680	
210	"	" 472	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS		REMARKS
R 211	Fixed Resistor	CR 25JU	222	
212	"	"	471	
213	"	"	680	
214	"	"	750	
215	"	"	681	
216	"	"	680	
217	"	"	472	
218	"	"	222	
219	"	"	"	
220	"	"	"	
221	"	"	"	
222	"	"	"	
223	"	"	"	
224	"	"	"	
225	"	"	331	
226	"	"	472	
227	"	"	222	
228	"	"	332	
229	"	"	101	
230	"	"	182	
231	"	"	471	
232	"	"	332	
233	"	"	152	
234	"	"	332	
235	"	"	101	
236	"	"	182	
237	"	"	361	
238	"	"	680	
239	"	"	361	
240	"	"	911	

SYMBOL	PART NAME	DESCRIPTIONS		REMARKS
R 241	Fixed Resistor	CR 25JU	681	
242	"	"	680	
243	"	"	182	
244	"	"	"	
245	"	"	221	
246	"	"	102	
247	"	"	680	
248	"	"	332	
249	"	"	680	
250	"	"	621	
251	"	"	102	
252	"	"	680	
253	"	"	471	
254	"	"	681	
255	"	"	680	
256	"	"	152	
257	"	"	"	
258	"	"	222	
259	"	"	182	
260	"	"	560	
261	"	"	103	
262	"	"	"	
263	"	"	"	
264	"	"	331	
265	"	"	472	
266	"	"	222	
267	"	"	182	
268	"	"	331	
269	"	"	680	
270	"	"	391	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS		REMARKS
R 271	Fixed Resistor	CR 25JU	182	
272	"	"	561	
273	"	"	103	
274	"	"	332	
275	"	"	"	
276	"	"	"	
277	"	"	101	
278	"	"	271	
279	"	"	182	
280	"	"	471	
281	"	"	102	
282	"	"	103	
283	"	"	102	
284	"	"	681	
285	"	"	101	
286	"	"	182	
287	"	"	"	
288	"	"	682	
289	"	"	302	
290	"	"	122	
291	"	"	105	
292	"	"	331	
293	"	"	122	
294	"	"	102	
295	"	"	103	
296	"	"	680	
297	"	"	332	
298	"	"	222	
299	"	"	182	
300	"	"	331	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS		REMARKS
R 301	Fixed Resistor	CR 25JU	391	
302	"	"	680	
303	"	"	182	
304	"	"	561	
305	"	"	103	
306	"	"	332	
307	"	"	"	
308	"	"	"	
309	"	"	101	
310	"	"	271	
311	"	"	182	
312	"	"	271	
313	"	"	471	
314	"	"	102	
315	"	"	103	
316	"	"	222	
317	"	"	152	
318	"	"	151	
319	"	"	472	
320	"	"	911	
321	"	"	221	
322	"	"	471	
323	"	"	221	
324	"	"	"	
325	"	"	681	
326	"	"	102	
327	"	"	"	
328	"	"	222	
329	"	"	221	
330	"	"	821	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS		REMARKS
R 331	Fixed Resistor	CR 25JU	680	
332	"	"	102	
333	"	"	272	
334	"	"	222	
335	"	"	680	
336	"	"	561	
337	"	"	102	
338	"	"	182	
339	"	"	152	
340	"	"	102	
341	"	"	182	
342	"	"	472	
343	"	"	752	
344	"	"	680	
345	"	"	222	
346	"	"	471	
347	"	"	122	
348	"	"	332	
349	"	"	272	
350	"	"	331	
351	"	"	561	
352	"	"	102	
353	"	"	182	
354	"	"	"	
355	"	"	"	
356	"	"	182	
357	"	"	331	
358	"	"	222	
359	"	"	103	
360	"	"	222	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS		REMARKS
C 361	Fixed Resistor	CR 25JU	361	
362	"	"	122	
363	"	"	511	
364	"	"	221	
365	"	"	822	
366	"	"	102	
367	"	"	332	
368	"	"	"	
369	"	"	102	
370	"	"	222	
371	"	"	332	
372	"	"	101	
373	"	"	102	
374	"	"	103	
375	"	"	102	
376	"	"	471	
377	"	"	102	
378	"	"	471	
379	"	"	332	
380	"	"	103	
381	"	"	101	
382	"	"	332	
383	"	"	101	
384	"	"	332	
385	"	"	102	
386	"	"	332	
387	"	"	822	
388	"	"	680	
389	"	"	152	
390	"	"	680	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS		REMARKS
R 391	Fixed Resistor	CR 25JU	680	
392	"	"	472	
393	"	"	681	
394	"	"	104	
395	"	"	102	
396	"	"	683	
397	"	"	102	
RA 1	Group Resistor	899-1-R	10K	
VR 1	Variable Resistor	GFP 06	102	
2	"	"	202	
3	"	"	"	
4	"	GFP 062	103	
5	"	GFP 06	102	
6	"	"	104	
7	"	"	502	
8	"	"	"	
9	"	"	"	
10	"	"	302	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS		REMARKS
VR 11	Variable Resistor	GFP 06	501	
12	"	Deleted		
13	"	GFP 06	102	
14	"	"	201	
15	"	"	501	
16	"	"	"	
17	"	"	102	
18	"	"	501	
19	"	"	102	
20	"	"	201	
21	"	"	501	
22	"	"	501	
23	"	"	501	
24	"	"	502	
25	"	"	102	
26	"	"	"	
27	"	"	501	
28	"	"	"	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 1	Electrolytic	16R 100	
2	Stacking Ceramic	2222 637 52688	
3	Film	CQ 92 1H 103	
4	Dip Mica	DM 331J	
5	Electrolytic	6.3R 221	
6	Film	CQ 92 1H 103	
7	"	"	
8	Stacking Ceramic	RPE 122C 104Z 50	
9	"	"	
10	Dip Mica	DM 471J	
11	"	DM 221J	
12	Tantal	1μF 35V	
13	Stacking Ceramic	RPE 122C 104Z 50	
14	Film	CQ 92 1H 103	
15	"	" 472	
16	Ceramic	104Z	
17	Film	CQ 92 1H 102	
18	"	" "	
19	"	" 152	
20	"	" 222	
21	"	" 103	
22	"	" 102	
23	Dip Mica	DM 101J	
24	Stacking Ceramic	RPE 122C 104Z 50	
25	Film	CQ 92 1H 682	
26	Dip Mica	DM 121J	
27	Film	CQ 92 1H 102	
28	Dip Mica	DM 750J	
29	Dip Mica	" 390J	
30	Dip Mica	" 151J	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 31	Dip Mica	MD 471J	
32	"	" 221J	
33	"	" 151J	
34	Film	CQ 92 1H 102	
35	"	" 103	
36	"	" 102	
37	Dip Mica	DM 470J	
38	"	" 101J	
39	"	" "	
40	"	" 561J	
41	Stacking Ceramic	RPE 122C 104Z 50	
42	Dip Mica	DM 561J	
43	Stacking Ceramic	RPE 122C 104Z 50	
44	Dip Mica	DM 470J	
45	Tantal	1μF 35V	
46	Dip Mica	DM 390J	
47	Film	CQ 92 1H 222	
48	Tantal	2.2μF 35V	
49	"	"	
50	Film	CQ 92 1H 103	
51	"	" 104	
52	"	" 102	
53	Stacking Ceramic	RPE 122C 104Z 50	
54	Film	CQ 92 222	
55	"	" 102	
56	Select		
57	Stacking Ceramic	RPE 122C 104Z 50	
58	Dip Mica	DM 680J	
59	Polystyrol	CQ 09S 2B 100J	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 60	Film	CQ 92 1M 102	
61	Dip Mica	DM 331J	
62	Tantal	1μF 35V	
63	"	"	
64	"	"	
65	Film	CQ 921H 103	
66	Stacking Ceramic	2222 637 52688	
67	Tantal	1μF 35V	
68	"	"	
69	Stacking Ceramic	2222-636-58339	
70	Polystyrol	CQ 09S C 1H 680J	
71	Film	CQ 92 1H 103	
72	"	" 102	
73	Stacking Ceramic	RPE 122C 104Z 50	
74	Dip Mica	DM 151J	
75	"	" 200J	
76	Film	CQ 92 1H 103	
77	Stacking Ceramic	RPE 122C 104Z 50	
78	Film	CQ 92 1H 152	
79	"	" 472	
80	"	" 222	
81	"	" 152	
82	Tantal	1μF 35V	
83	"	"	
84	Stacking Ceramic	2222-636-58339	
85	Dip Mica	DM 680J	
86	Film	CQ 92 1H 103	
87	Stacking Ceramic	RPE 122C 104Z 50	
88	Film	CQ 92 1H 104Z 102	
89	"	" 103	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 90	Film	CQ 92 1H 103	
91	Tantal	0.47μF 35V	
92	Film	CQ 92 1H 104	
93	"	" 222	
94	Dip Mica	DM 331J	
95	Film	CQ 92 1H 102	
96	Stacking Ceramic	RPE 122C 104Z 50	
97	Tantal	0.47μF 35V	
98	"	1μF 35V	
99	Electrolytic	16R 221	
100	"	"	
101	Film	CQ 92 1H 152	
102	"	" 102	
103	Dip Mica	DM 331J	
104	Electrolytic	16R 470	
105	Dip Mica	DM 101J	
106	"	" 010J	
107	Tantal	1μF 35V	
108	Stacking Ceramic	RPE 122C 104Z 50	
109	Dip Mica	DM 680J	
110	"	" 101J	
111	Dip Mica	DM 121J	
112	"	" 220J	
113	"	" 221J	
114	"	" 101J	
115	"	" 391J	
116	"	" 220J	
117	"	" 020J	
118	Tantal	1μF 35V	
119	Stacking Ceramic	RPE 122C 104Z 50	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 120	Dip Mica	DM 910J	
121	"	" 431J	
122	"	" 122J	
123	Tantal	0.47μF 35V	
124	Dip Mica	DM 471J	
125	Stacking Ceramic	RPE 122C 104Z 50	
126	"	"	
127	Film	CQ 92 1H 103	
128	Stacking Ceramic	RPE 122C 104Z 50	
129	"	"	
130	Film	CQ 92 1H 103	
131	Dip Mica	DM 680J	
132	Film	CQ 92 1H 102J	
133	Tantal	1μF 35V	
134	Dip Mica	DM 910J	
135	"	" 431J	
136	"	" 122J	
137	Tantal	0.47μF 35V	
138	Film	CQ 92 1H 102	
139	Stacking Ceramic	RPE 122C 104Z 50	
140	"	"	
141	Film	CQ 92 1H 223	
142	Electrolytic	6.3R 470	
143	Stacking Ceramic	RPE 122C 104Z 50	
144	"	"	
145	Film	CQ 92 1H 233	
146	"	" 102	
147	"	" 103	
148	Stacking Ceramic	RPE 122C 104Z 50	
149	Dip Mica	DM 680J	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 150	Stacking Ceramic	RPE 122C 104Z 50	
151	Electrolytic	16R 100	
152	Stacking Ceramic	RPE 122C 104Z 50	
153	"	2222 637 52688	
154	"	"	
155	Dip Mica	DM 470J	
156	"	" 101J	
157	Film	CQ 92 1H 333	
158	Stacking Ceramic	2222 637 52221	
159	Dip Mica	DM 820J	
160	Film	CQ 92 1H 102	
161	Electrolytic	6.3R 470	
162	Dip Mica	DM 471J	
163	Electrolytic	16R 100	
164	Stacking Ceramic	RPE 122C 104Z 50	
165	"	2222 636 58399	
166	"	" "	
167	Dip Mica	DM 101J	
168	"	" 561J	
169	"	Select	
170	"	DM 470J	
171	"	" 621J	
172	Stacking Ceramic	2222 637 58271	
173	Film	CQ 92 1H 103	
174	Stacking Ceramic	RPE 122C 104Z 50	
175	"	"	
176	Tantal	1μF 35V	
177	Stacking Ceramic	RPE 122C 104Z 50	
178	Electrolytic	16R 100	
179	Stacking Ceramic	RPE 122C 104Z 50	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 180	Stacking Ceramic	2222 637 52569	
181	Film	CQ 92 1H 103	
182	Dip Mica	DM 101J	
183	Film	CQ 92 1H 103	
184	Electrolytic	16R 470	
185	"	6.3R 101	
186	"	16R 470	
187	Select		
188	Dip Mica	DM 221J	
189	Select		
190	Stacking Ceramic	RPE 122C 104Z 50	
191	Deleted		
192	"		
193	"		
194	"		
195	"		
196	"		
197	"		
198	"		
199	"		
200	"		
201	Celamic	104Z	
202	"	"	
203	Electrolytic	16R 101	
204	Deleted		
205	"		
206	"		
207	"		
208	Stacking Ceramic	RPE 122C 104Z 50	
209	Ceramic	104Z	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 210	Stacking Ceramic	RPE 122C 104Z 50	
211	Ceramic	104Z	
212	Deleted		
213	"		
214	"		
215	Ceramic	104Z	
216	Electrolytic	16R 101	
217	Ceramic	104Z	
218	Electrolytic	16R 101	
219	Ceramic	104Z	
220	"	"	
221	Deleted		
222	"		
223	Ceramic	104Z	
224	Deleted		
225	Ceramic	104Z	
226	"	"	
227	"	"	
228	Electrolytic	16R 101	
229	Deleted		
230	Ceramic	104Z	
231	"	"	
232	Deleted		
233	Stacking Ceramic	RPE 122C 104Z 50	
234	Deleted		
235	Ceramic	104Z	
236	Deleted		
237	"		
238	Electrolytic	16R 101	
239	Ceramic	104Z	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 240	Electrolytic	16R 101	
241	Ceramic	104Z	
242	Electrolytic	16R 101	
243	Ceramic	104Z	
244	"	"	
245	"	"	
246	Deleted		
247	Ceramic	104Z	
248	Electrolytic	16R 101	
249	Deleted		
250	"		
251	Stacking Ceramic	RPE 122C 104Z 50	
252	"	"	
253	"	"	
254	Ceramic	104Z	
255	"	"	
256	"	"	
257	"	"	
258	Deleted		
259	Electrolytic	16R 101	
260	"	"	
261	Ceramic	104Z	
262	Electrolytic	16R 101	
263	Ceramic	104Z	
264	Deleted		
265	Ceramic	104Z	
266	Deleted		
267	Ceramic	104Z	
268	Electrolytic	16R 101	
269	Deleted		

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 270	Ceramic	104Z	
271	"	"	
272	"	"	
273	"	"	
274	Deleted		
275	"		
276	"		
277	"		
278	Ceramic	104Z	
279	"	"	
280	"	"	
281	Electrolytic	16R 101	
282	"	"	
283	Ceramic	104Z	
284	Deleted		
285	Ceramic	104Z	
286	Deleted		
287	Ceramic	104Z	
288	Deleted		
289	"		
290	"		
291	"		
292	Ceramic	104Z	
293	"	"	
294	"	"	
295	Deleted		
296	Ceramic	104Z	
297	Deleted		
298	"		
299	Ceramic	104Z	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 300	Deleted		
301	Stacking Ceramic	RPE 122C 104Z 50	
302	Deleted		
303	Ceramic	104Z	
304	"	"	
305	"	"	
306	"	"	
307	Deleted		
308	Electrolytic	16R 101	
309	Ceramic	104Z	
310	Deleted		
311	Electrolytic	16R 101	
312	Ceramic	104Z	
313	Deleted		
314	"		
315	Ceramic	104Z	
316	"	"	
317	"	"	
318	"	"	
319	"	"	
320	Deleted		
321	"		
322	"		
323	Electrolytic	16R 470	
324	Stacking Ceramic	RPE 122C 104Z 50	
325	Electrolytic	16R 470	
326	Stacking Ceramic	RPE 122C 104Z 50	
327	Ceramic	104Z	
328	Deleted		
329	"		

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 330	Ceramic	104Z	
331	"	"	
332	Electorlytic	16R 101	
333	Stacking Ceramic	RPE 122C 104Z 50	
334	Electrolytic	16R 101	
335	"	16R 470	
336	"	16R 101	
337	Ceramic	104Z	
338	"	"	
339	"	"	
340	"	"	
341	Deleted		
342	Ceramic	104Z	
343	Deleted		
344	"		
345	Electrolytic	16R 470	
346	Ceramic	104Z	
347	"	"	
348	Deleted		
349	Ceramic	104Z	
350	"	"	
351	"	"	
352	Deleted		
353	Ceramic	104Z	
354	"	"	
355	"	"	
356	"	"	
357	Deleted		
358	"		
359	Electrolytic	16R 101	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 360	Ceramic	104Z	
361	Electrolytic	16R 101	
362	Ceramic	104Z	
363	Deleted		
364	"		
365	Electrolytic	16R 331	
366	Ceramic	104Z	
367	Electrolytic	16R 331	
368	Ceramic	104Z	
369	Electrolytic	16R 331	
370	Ceramic	104Z	
371	Electrolytic	16R 331	
372	Ceramic	104Z	
373	Electrolytic	6.3R 471	
374	Ceramic	104Z	
375	Electrolytic	6.3R 471	
376	Ceramic	104Z	
377	"	"	
378	Deleted		
379	Ceramic	104Z	
380	"	"	
381	Electrolytic	16R 470	
382	Ceramic	104Z	
383	"	"	
384	"	"	
385	"	"	
386	"	"	
387	"	"	
388	Deleted		
389	"		

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 390	Electrolytic	16R 101	
391	Ceramic	104Z	
392	"	"	
393	Electrolytic	16R 101	
394	Deleted		
395	Ceramic	104Z	
396	"	"	
397	"	"	
398	"	"	
399	"	"	
400	"	"	
401	"	"	
402	"	"	
403	"	"	
404	"	"	
405	"	"	
406	"	"	
407	"	"	
408	"	"	
409	"	"	
410	"	"	
411	"	"	
412	"	"	
413	"	"	
414	"	"	
415	"	"	
416	Deleted		
417	Ceramic	104Z	
418	"	"	
419	"	"	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 420	Ceramic	104Z	
421	"	"	
422	"	"	
423	"	"	
424	"	"	
425	"	"	
426	"	"	
427	"	"	
428	"	"	
429	"	"	
430	"	"	
431	"	"	
432	"	"	
433	"	"	
434	"	"	
435	"	"	
436	"	"	
437	"	"	
438	"	"	
439	"	"	
440	"	"	
441	"	"	
442	"	"	
443	"	"	
444	"	"	
445	"	"	
446	"	"	
447	"	"	
448	"	"	
449	"	"	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
C 450	Ceramic	104Z	
451	Electrolytic	6.3R 101	
452	"	6.3R 471	
453	Ceramic	104Z	
454	Electrolytic	6.3R 101	
455	Ceramic	104Z	
456	Electrolytic	6.3R 101	
457	"	6.3R 101	
458	Ceramic	104Z	
459	Electrolytic	6.3R 101	
460	"	6.3R 101	
461	Ceramic	104Z	
462	Electrolytic	6.3R 101	
463	Deleted		
464	"		
465	Ceramic	104Z	
466	"	"	
C467~500	Deleted		
C 501	Stacking Ceramic	RPE 122C 104Z 50	
502	"	"	
503	Ceramic	104Z	
504	"	"	
505	"	"	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
VC 1	Variable Condenser	ECV-1ZW 25X 53N	
2	"	"	
3	Deleted	ECV-1ZW 20 X 53N	
4	Variable Condenser	ECV-1ZW 20 X 53N	
5	"		
L 1	Deleted		
2	Inductance	FL9H 100M	
3	"	" "	
4	"	" "	
5	"	" "	
6	Variable Inductance	P-0104	
7	Inductance	FL 5H 470K	
8	"	" 101K	
9	"	" 100K	
10	"	" 151K	
11	Variable Inductance	P-0075	
12	"	P-0076	
13	Inductance	FS 0712-220K	
14	Variable Inductance	P-0076	
15	Deleted		

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
L 16	Inductance	FL 5H 220K	
17	"	" 150K	
18	"	" 100K	
19	"	" 470K	
20	"	" 390K	
21	"	" 820K	
22	"	" 390K	
23	"	" 820K	
24	Variable Inductance	P-0103	
25	"	FS 0712-220K	
26	"	FS 0712-6R 8	
27	"	FL 4H 2R 7M	
28	Variable Inductance	P-0104	
RGE 1	Regulater	LM 79 L 05A	
2	"	μA 78 L 62 AC	
3	"	"	
4	"	LM 79 L 05A	
X-tal 1	Oscillator	P-0040	
2	"	"	

FA-410N OUTPUT PROCESSOR BAORD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
RL-1	Relay	DIP-1T05	
"	Socket	14 Pin	
RL-2	Relay	DIP-1T05	
"	Socket	14 Pin	
DSW 1	Dip Switch	A6 MS-4	
" 2	"	" -4	
" 3	"	" -8	
J 1	Housing	IL-G-6S-53C2	
"	Terminal	IL-G-6P-S3T2-E	
J 2	Plathome	IC-31-14	
"	Plate	for IC-31-14	
J 3	Plathome	IC-31-14	
"	Plate	for IC-31-14	
J 4		IL-G-10S-S3C2	
"	Terminal	IL-G-10P-S3T2-E	
J 5		IL-G-11S-S3C2	
"	Terminal	IL-G-11P-S3T2-E	
J 6		IL-G-9S-S3C2	
"	Terminal	IL-G-9P-S3T2-B	
J 7		IL-G-7S-S3C2	
"	Terminal	IL-G-7P-S3T2-E	
J 8	Connector	TN-50P-06-L1	
"		TN-50H-06-A1	
"	Terminal	004T-4100	
J 9	Connector	TN-50P-03-L1	
"		TN-50H-03-A1	
"	Terminal	004T-4100	

FA-410N OUTPUT PROCESSOR BOARD

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
TP1 18	Test Pin	LC1-S	
GND	Ground Test Pin	FTR-45-115	
JP 5	Jumper Pin	MINI JUMP 65474	
"	Jumper Head	STREAT HEAD 6550-208	

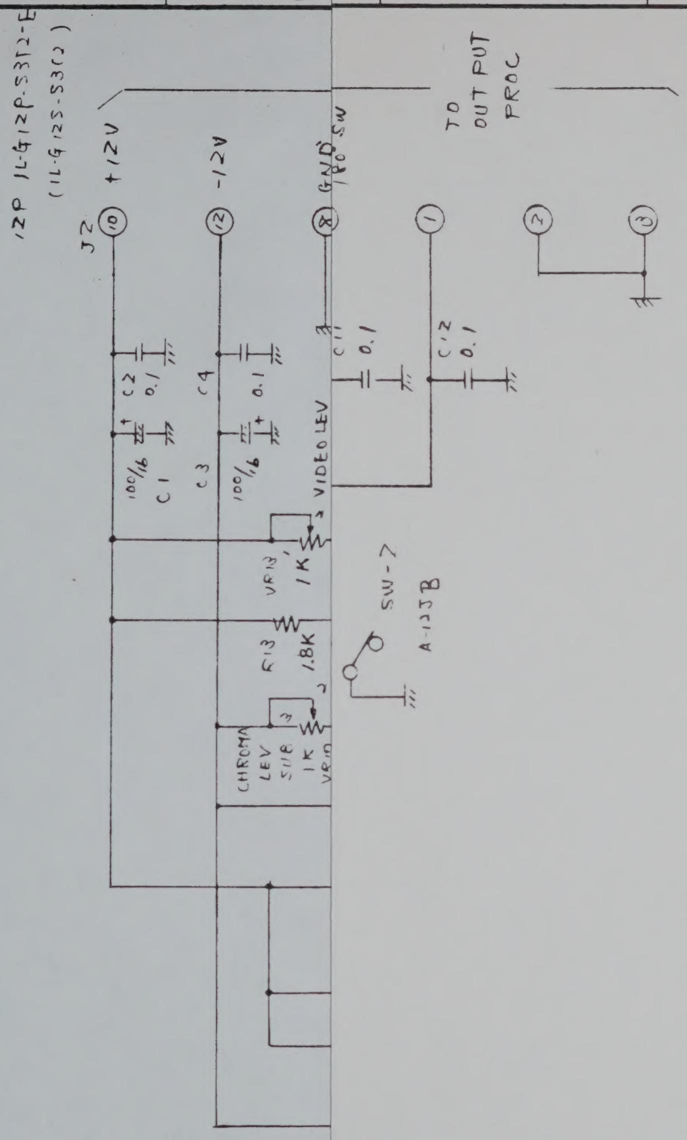
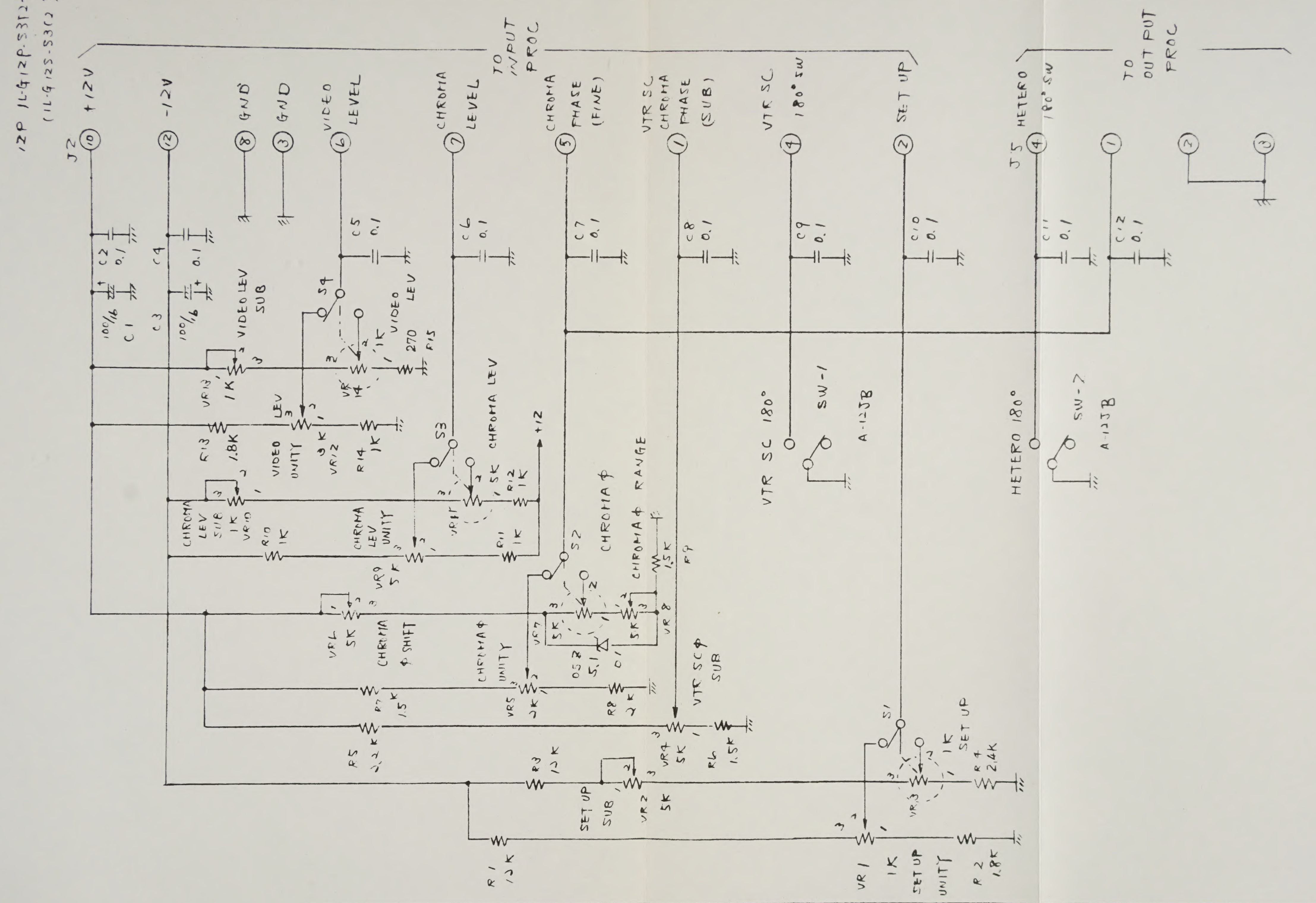

12P IL-G12P-S3T2-E
(IL-G12S-S3(2))
J2
+12V
-12V
GND 180° SW
TO OUT PUT PROC
10
12
8
1
2
3
C2 0.1
C1 100/16
C4 0.1
C3 100/16
C11 0.1
C12 0.1
VIDEO LEV
VR13 1K
R13 1.8K
SW-7
A-123B
CHROMA LEV SUB 1K VR10

図	承認	図名
C	沢口	FA410 N OPERATION PANEL PCB 1/2

図番	部番
A3. 2811-1	

株式会社 朋栄

FOR.A


12P JL-G12P-S3T2-E
(JL-G12S-S3(2))
J2
⑩ +12V
⑫ -12V
⑧ GND
③ GND
⑥ VIDEO LEVEL
⑦ CHROMA LEVEL
TO INPUT PROC
⑤ CHROMA PHASE (FINE)
① VTR SC CHROMA PHASE (SUB)
④ VTR SC 180° SW
② SET UP
J5
④ HETERO 180° SW
①
②
③
TO OUT PUT PROC
C1 100/16
C2 0.1
C3 100/16
C4 0.1
C5 0.1
C6 0.1
C7 0.1
C8 0.1
C9 0.1
C10 0.1
C11 0.1
C12 0.1
S4
VIDEO LEV SUB
VR13 1K
VR14 1K VIDEO LEV
270 R15
R13 1.8K
VIDEO UNITY VR12 3K LEV
R14 1K
S3
CHROMA LEV
+12
VR11 1.5K
R12 1K
CHROMA LEV SUB 1K VR10
R10 1K
CHROMA LEV UNITY VR9 5K
R11 1K
S2
CHROMA φ
CHROMA φ RANGE
R9 1.5K
VR6 5K
CHROMA φ SHIFT
VR7 5K
VR8 5K
05Z 5.1
D1
CHROMA φ UNITY
VR5 3K
R7 1.5K
R8 2K
VTR SC φ SUB
R5 2.2K
VR4 5K
R6 1.5K
R3 12K
SET UP SUB
VR2 5K
R1 12K
S1
VR3 1K SET UP
R4 2.4K
VR1 1K SET UP UNITY
R2 1.8K
VTR SC 180°
SW-1
A-12JB
HETERO 180°
SW-7
A-12JB
1 2 3 4 5 6 7 8
A B C D E F

改訂	A

第三角図法	製図	設計	検図	承認	図名
尺度 ／	A.N	A.K	I.C		FA410 N OPERATION PANEL PCB 1/2
作成 年 月 日	製番		図番		部番
個数			A3. 2811-1		

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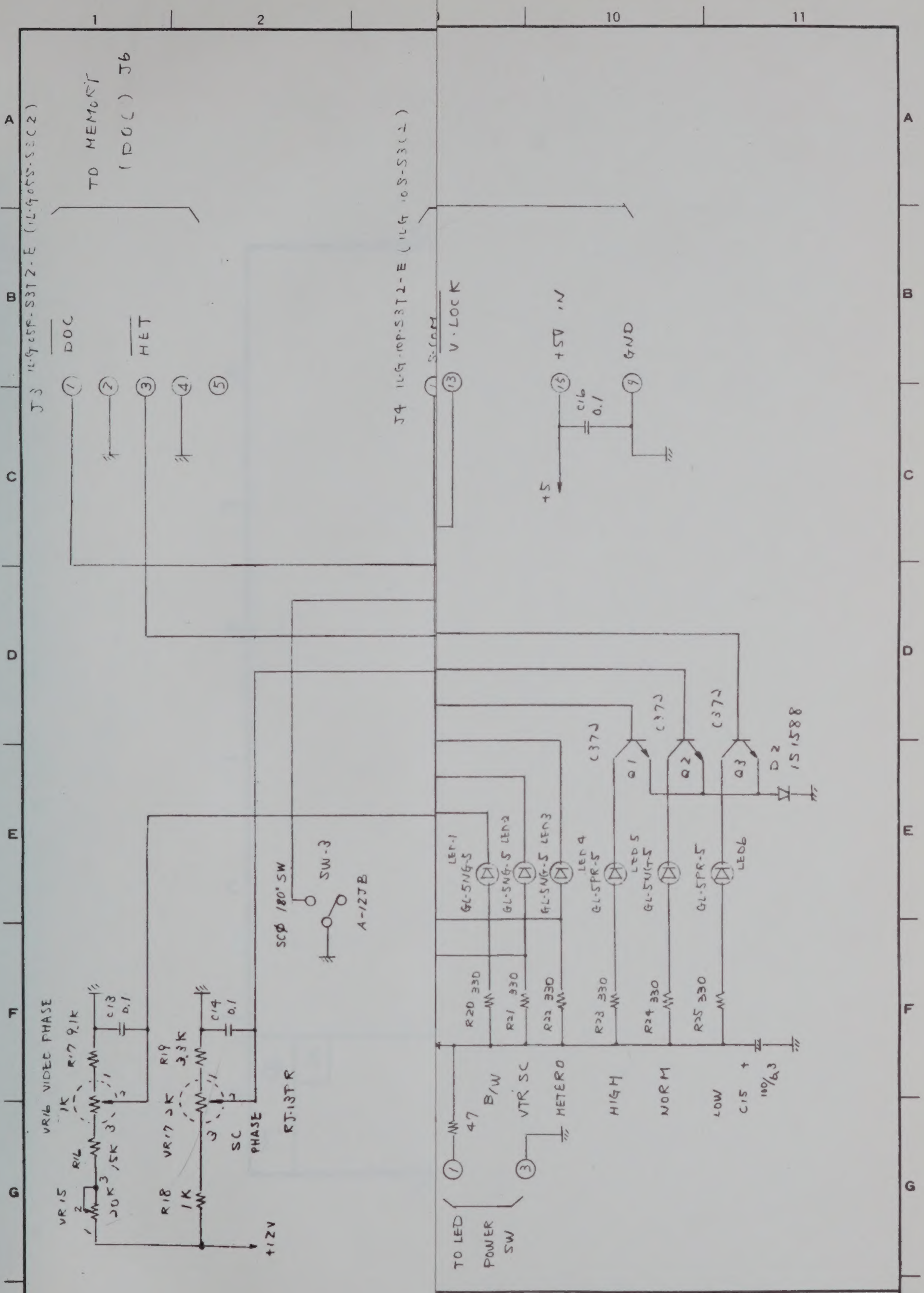
TO MEMORY
(DOC) J6
J3 IL-G-05P-S3T2-E (IL-G-05S-S3C(2))
DOC
HET
①
②
③
④
⑤
J4 IL-G-10P-S3T2-E (IL-G-10S-S3C(2))
S-COM
V·LOCK
⑬
⑮
+5V IN
⑨
GND
C16
0.1
+5
(37J)
Q1
(37J)
Q2
(37J)
Q3
D2
1S1588
SCØ 180° SW
SW-3
A-12JB
LED-1
GL-5NG-5
GL-5NG-5 LED2
GL-5NG-5 LED3
LED4
GL-5PR-5
LED5
GL-5UG-5
GL-5PR-5
LED6
R20 330
R21 330
R22 330
R23 330
R24 330
R25 330
47
B/W
VTR SC
HETERO
HIGH
NORM
LOW
C15 +
100/6.3
①
③
TO LED
POWER
SW
VR16 VIDEO PHASE
1K
R17 9.1K
C13
0.1
R16
15K
VR15
20K
R19
3.3K
C14
0.1
VR17 2K
SC
PHASE
RJ-13TR
R18
1K
+12V
1
2
9
10
11
A
B
C
D
E
F
G
H

法	製図	設計	検図	承認	図名
/	A.N	A.K	10	永园	FA410 N OPERATION PANEL PCB 2/2

月 日	製番	図番	部番
		A2-3439-1	

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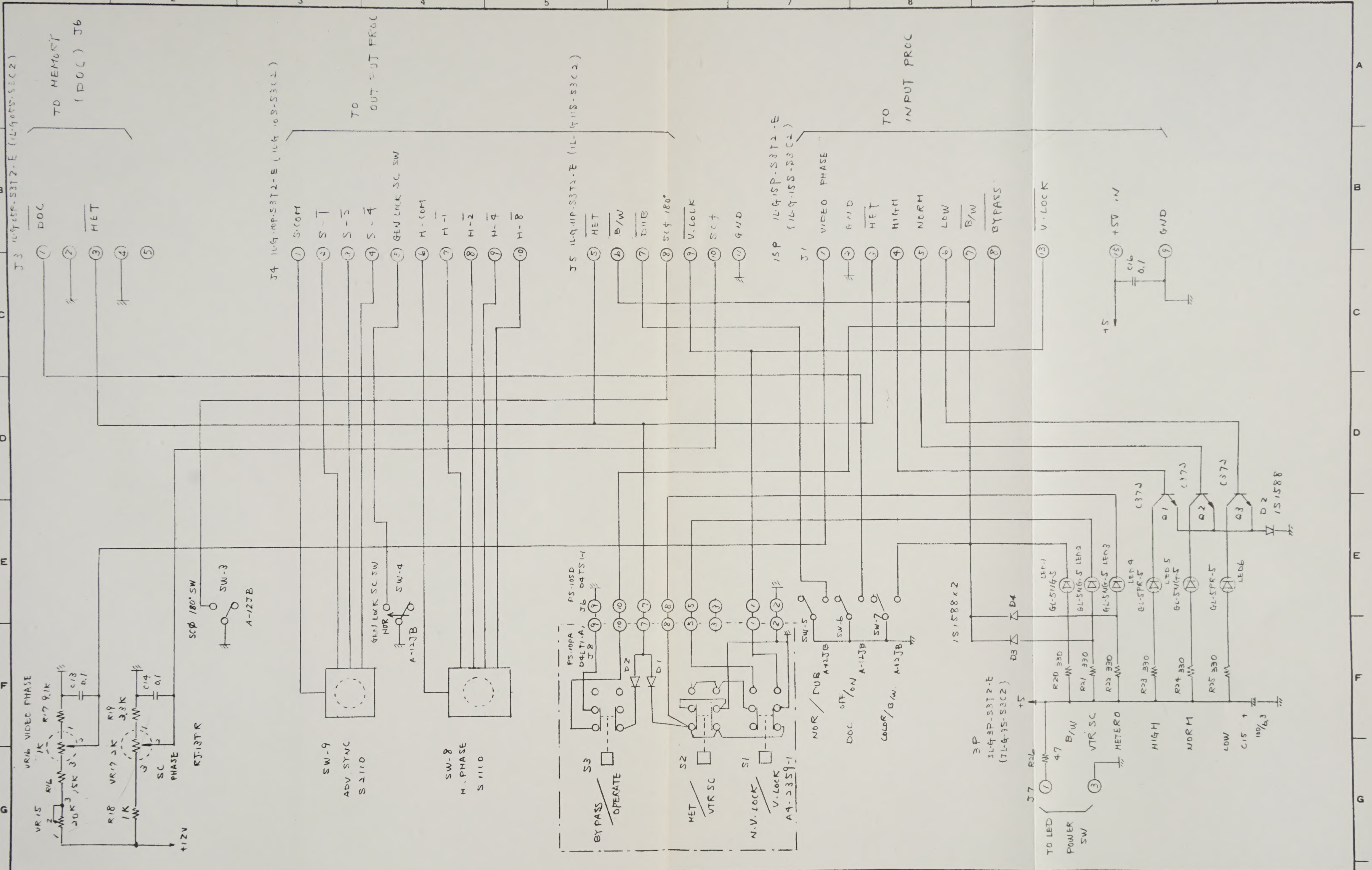
FOR.A


TO MEMORY (DOC) J6
J3 IL-G-05P-S3T2-E (IL-G-05S-S3C2)
DOC
HET
TO OUT PUT PROC
J4 IL-G-10P-S3T2-E (IL-G-10S-S3C2)
S-COM
S-1
S-2
S-4
GEN LOCK SC SW
H-COM
H-1
H-2
H-4
H-8
J5 IL-G-11P-S3T2-E (IL-G-11S-S3C2)
HET
B/W
DUB
SC¢ 180°
V.LOCK
SC¢
GND
TO INPUT PROC
15P IL-G-15P-S3T2-E (IL-G-15S-S3C2)
J1
VIDEO PHASE
GND
HET
HIGH
NORM
LOW
B/W
BYPASS
V.LOCK
+5V IN
GND
C16 0.1
+5
(37J)
Q1
Q2
Q3
D2 1S1588
SCØ 180° SW
SW-3
A-12JB
GEN LOCK SC SW
NOR
SW-4
A-12JB
VR16 VIDEO PHASE
R17 9.1K
C13 0.1
1K
R16 15K
VR15 20K
R19 3.3K
C14 0.1
VR17 2K
SC PHASE
R18 1K
+12V
RJ-13TR
SW-9 ADV SYNC S2110
SW-8 H.PHASE S1110
PS-10PA D4LT1-A, J8
PS-10SD D4TS1-1 J6
D2
D1
S3 BYPASS / OPERATE
S2 HET / VTR SC
S1 N.V. LOCK / V.LOCK
A4-2359-1
SW-5 NOR / DUB A-12JB
SW-6 OFF / ON DOC A-12JB
SW-7 COLOR / B/W A-12JB
1S1588 x 2
D4
D3
LED-1 GL-5NG-5
GL-5NG-5 LED2
GL-5NG-5 LED3
LED4 GL-5PR-5
LED5 GL-5UG-5
GL-5PR-5 LED6
R20 330
R21 330
R22 330
R23 330
R24 330
R25 330
+5
3P IL-G-3P-S3T2-E (IL-G-3S-S3C2)
R26 47
B/W
VTR SC
HETERO
HIGH
NORM
LOW
C15 100/6.3
J7
TO LED POWER SW

改訂	A	第三角図法		製図	設計	検図	図名
		尺度	/	A.N	AK	10	FA410 N OPERATION PANEL PCB 2/2
		作成 年 月 日		製番		図番 A2-3439-1	部番
		個数					

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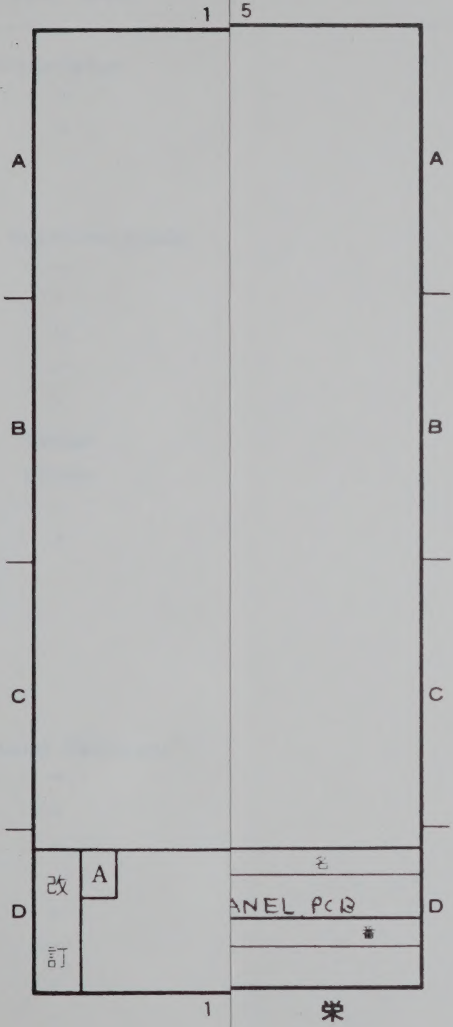
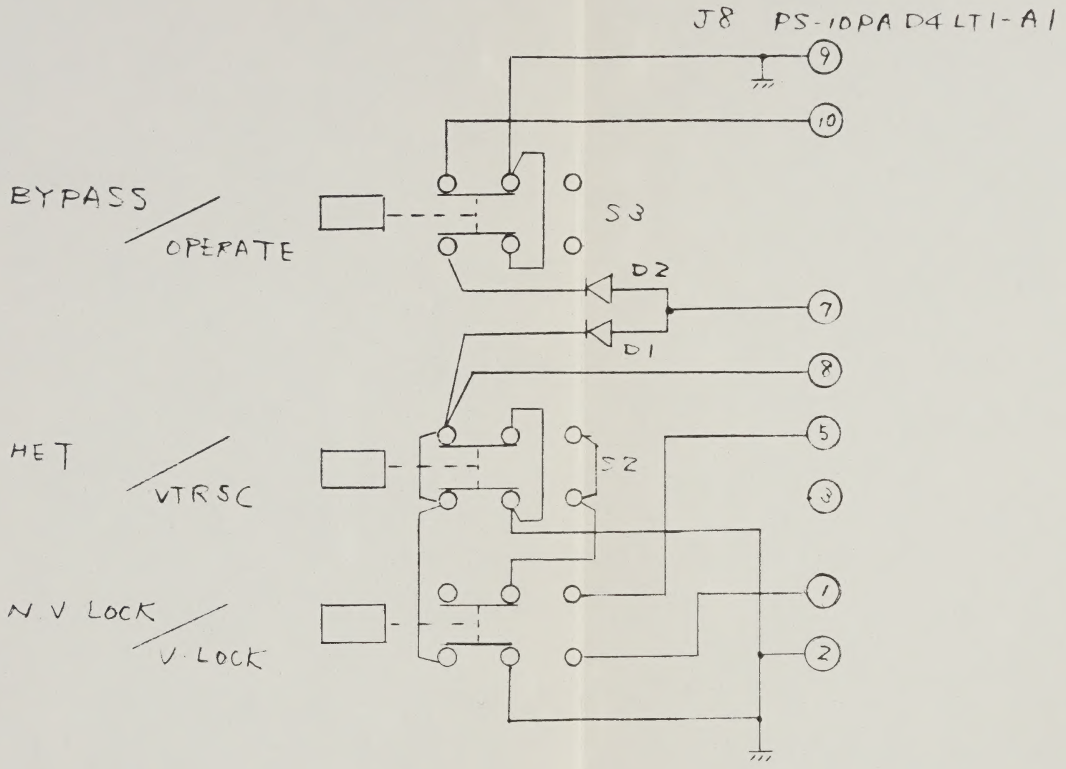

1
5
A
A
B
B
C
C
D
D
改
訂
A
名
ANEL PCB
番
1
栄


J8 PS-10PA D4 LT1-A1
9
10
BYPASS
OPERATE
S3
D2
7
D1
8
HET
VTRSC
S2
5
3
N.V LOCK
V.LOCK
1
2

改訂 A

第三角図法	製図	設計	検図	承認	図名
尺度 /					FA 410N SW PANEL PCB
作成　年　月　日	製番		図番		部番
個数			A4 2359-1		

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FA-410N OPERATION PANEL

A2-3439-2~A3-2811-2

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
Q 1	Transistor	2 SC 372	
2	"	"	
3	"	"	
LED 1	Light Emission Diode	GL 5NG-5	
2	"	"	
3	"	"	
4	"	GL 5NR-5	
5	"	GL 5NG-5	
6	"	GL 5NR-5	
D 1	Zener	05Z 5.1	
2	Diode	IS 1588	
3	"	"	
4	"	"	
R 1	Fixed Resistor	CR 25J 123	
2	"	" 182	
3	"	" 123	
4	"	" 242	
5	"	" 222	
6	"	" 152	
7	"	" "	
8	"	" 202	
9	"	" 152	
10	"	" 102	

FA-410N OPERATION PANEL

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
R 11	Fixed Resistor	CR 25J 102	
12	"	" "	
13	"	" 182	
14	"	" 102	
15	"	" 271	
16	"	" 153	
17	"	" 682	
18	"	" 102	
19	"	" 332	
20	"	" 331	
21	"	" "	
22	"	" "	
23	"	" "	
24	"	" "	
25	"	" "	
26	"	" 470	
VR 1	Variable Resistor	GFP 06 102	
2	"	" 502	
3	"	V16L4S(SL123) 1KΩ	
4	"	GFP 06 502	
5	"	" 202	
6	"	" 502	
7	"	V16L4S(SL123)5KΩ	
8	"	GFP 06 502	
9	"	" "	
10	"	" 102	

FA-410N OPERATION PANEL

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
VR 11	Variable Resistor	V16L4S(SL123) 5KΩ	
12	"	GFP 06 102	
13	"	" "	
14	"	V10L4S(SL123) 1KΩ	
15	"	GFP06 203	
16	"	RJ13PR 102	
17	"	" 202	
C 1	Electrolytic	16R 101	
2	Ceramic	104Z	
3	Electrolytic	16R 101	
4	Ceramic	104Z	
5	"	"	
6	"	"	
7	"	"	
8	"	"	
9	"	"	
10	"	"	
11	"	"	
12	"	"	
13	"	"	
14	"	"	
15	Electrolytic	6.3R 101	
16	Ceramic	104Z	
17	"	"	
18	"	6.3R 101	
L 1	Inductance	FL7H 101	

FA-410N OPERATION PANEL

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
SW 1	Switch	A-12JB	
2	"	"	
3	"	"	
4	"	"	
5	"	"	
6	"	"	
7	"	"	
8	"	S 1110	
9	"	S 2110	
J 1	Connector	ILG-15P-S3T2-E	
2	"	ILG-12P-S3T2-E	
3	"	ILG-05P-S3T2-E	
4	"	ILG-10P-S3T2-E	
5	"	ILG-11P-S3T2-E	
6	"	PS 10 PA 04R1-A1	
7	"	ILG-03P-S3T2-E	
J 1	Housing	IL-15S-S3L	
2	"	IL-12S-S3L	
3	"	IL-05S-S3L	
4	"	IL-10S-S3L	
5	"	IL-11S-S3L	
6	"	PS-10SD D4TS 1-1	
7	"	IL-03S-S3L	
	Fuse holder for spare	F-3265	
	Fuse for spare	UL. CSA 6.3×32 SLO-BLO 3A	

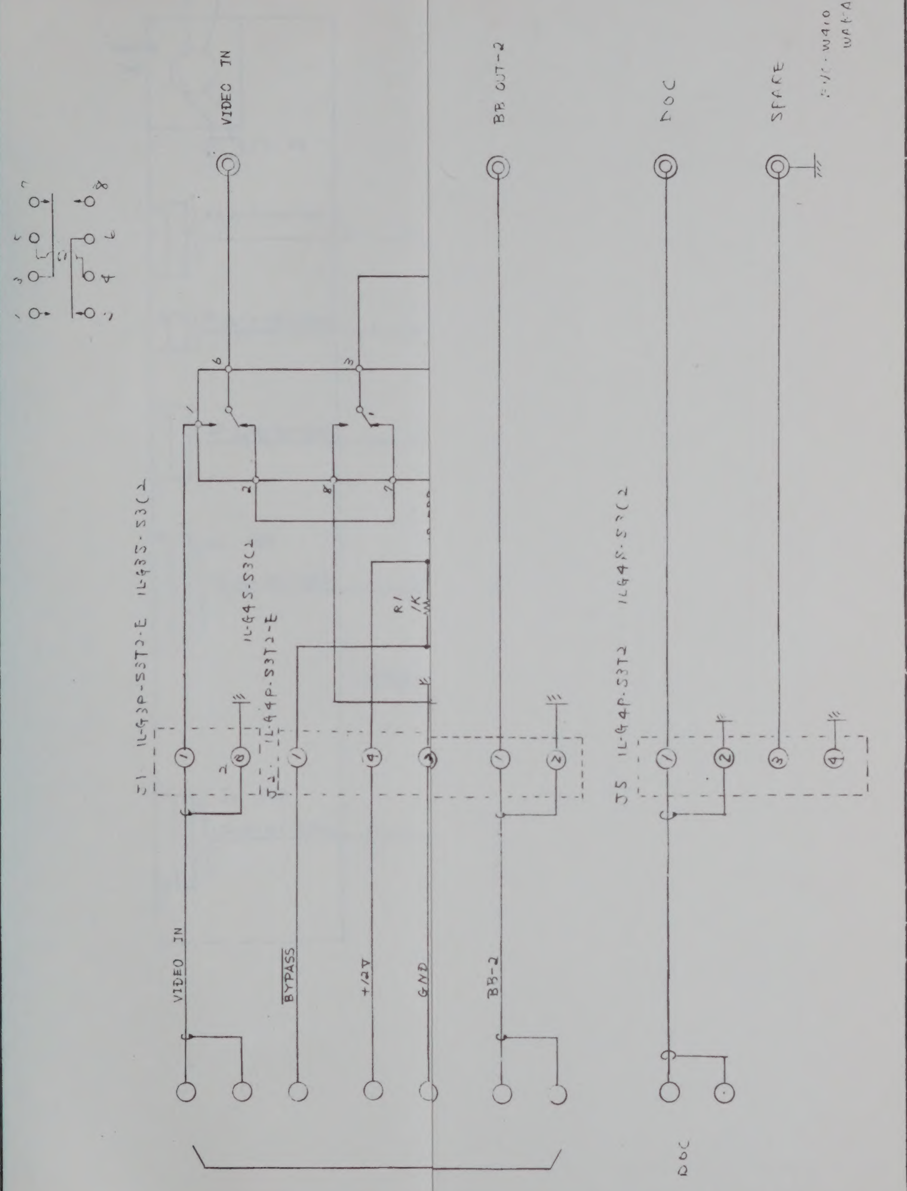
FA-410N FRONT PANEL

1/1

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
D 1	Diode	IS 1588	
2	"	"	
S 1	Triplet Switch	P-0070	
2			
3			
J1~7	Deleted		
J 8	Connector	PS 10 PAD 4 LT1-A1	
J1~7	Deleted		
J 8	Housing	PS-10SD D4TS1-1	

FA-410N OPERAITON PANEL

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
Q 1	Transistor	2 SC 594	
D 1	Diode	IS 1588	
R 1	Fixed Resistor	CR 25J 102	
2	"	" 331	
3	"	" 472	
C 1	Ceramic	104Z	
RL 1	Relay	CM 04-A1 BD	
J 1	Connector	ILG 3P-S3T2-E	
2	"	ILG 4P-S3T2-E	
3	"	ILG 8P-S3T2-E	
4	"	ILG 9P-S3T2-E	
5	"	ILG 4P-S3T2-E	
J 1	Housing	IL-3S-S3C2	
2	"	IL-4S-S3C2	
3	"	IL-8S-S3C2	
4	"	IL-9S-S3C2	
5	"	IL-4S-S3C2	
BNC Connector		BNC-W410	


VIDEO IN
BB OUT-2
DOC
SPARE
SW·W410
WAKA
J1 IL-G3P-S3T2-E
IL-G3S-S3C2
J2 IL-G4P-S3T2-E
IL-G4S-S3C2
R1
1K
J5 IL-G4P-S3T2
IL-G4S-S3C2
VIDEO IN
BYPASS
+12V
GND
BB-2
DOC

法	製図	設計	検図	承認	図名
/	山下	AK	10	文	FA410 N CONNECTOR BOARD
日	製番		図番		部番
			A2-3438-1		

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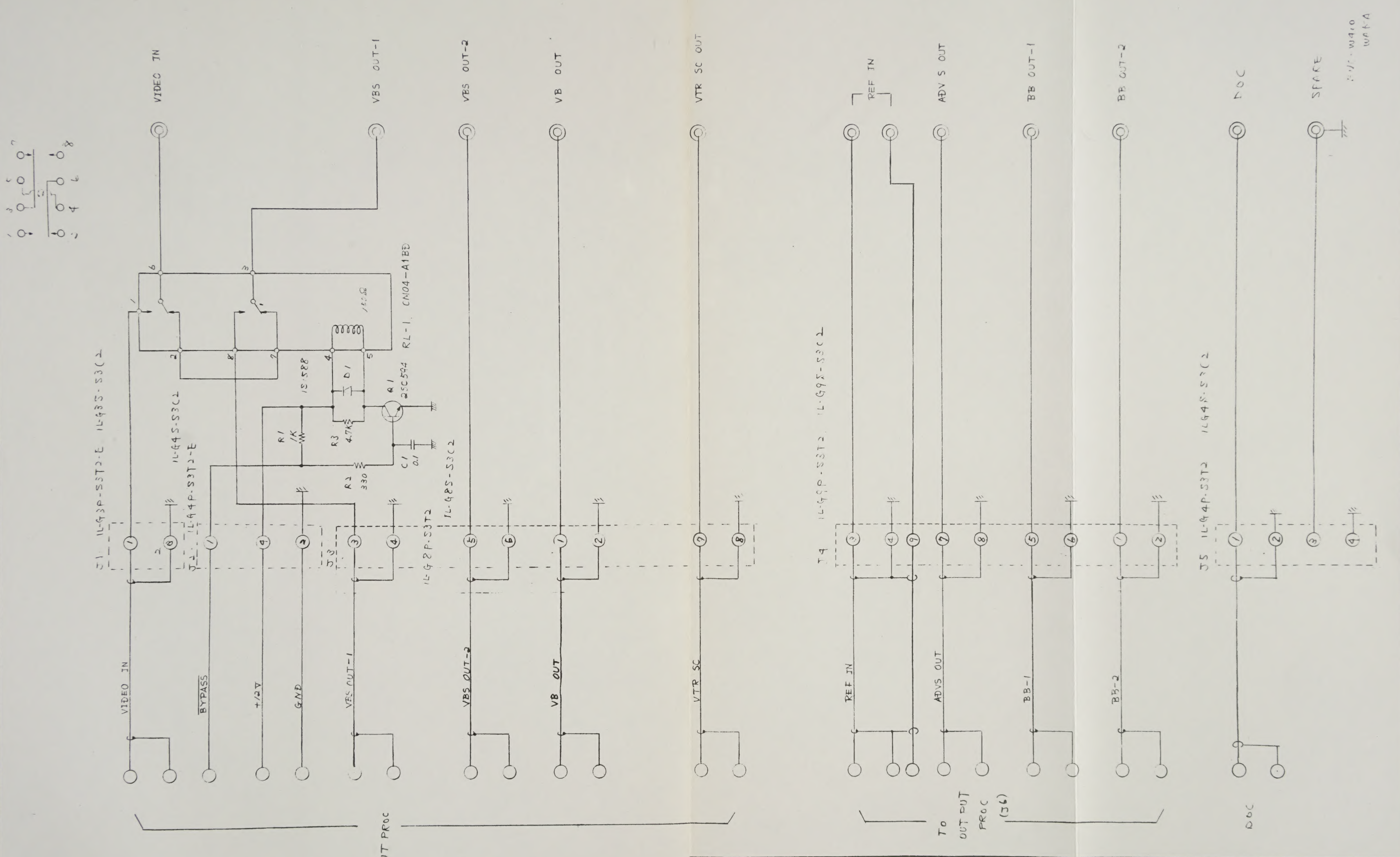
FOR.A


VIDEO IN
VBS OUT-1
VBS OUT-2
VB OUT
VTR SC OUT
REF IN
ADV S OUT
BB OUT-1
BB OUT-2
DOC
SPARE
F.V.·W410 WAKA
RL-1 CN04-A1BD
150Ω
1S1588
D1
Q1
2SC594
R1
1K
R3
4.7K
R2
330
C1
0.1
IL-G3P-S3T2-E
IL-G3S-S3C2
IL-G4S-S3C2
IL-G4P-S3T2-E
IL-G8S-S3C2
IL-G8P-S3T2
IL-G9P-S3T2
IL-G9S-S3C2
IL-G4P-S3T2
IL-G4S-S3C2
J1
J2
J3
J4
J5
VIDEO IN
BYPASS
+12V
GND
VBS OUT-1
VBS OUT-2
VB OUT
VTR SC
REF IN
ADVS OUT
BB-1
BB-2
To INPUT PROC
To OUT PUT PROC (J6)
DOC

改訂	A

第三角図法	製図	設計	検図	承認	図名
尺度 /	山下	AK	10	文日	FA410 N CONNECTOR BOARD
作成 年 月 日	製番			図番	部番
個数				A2·3438-1	

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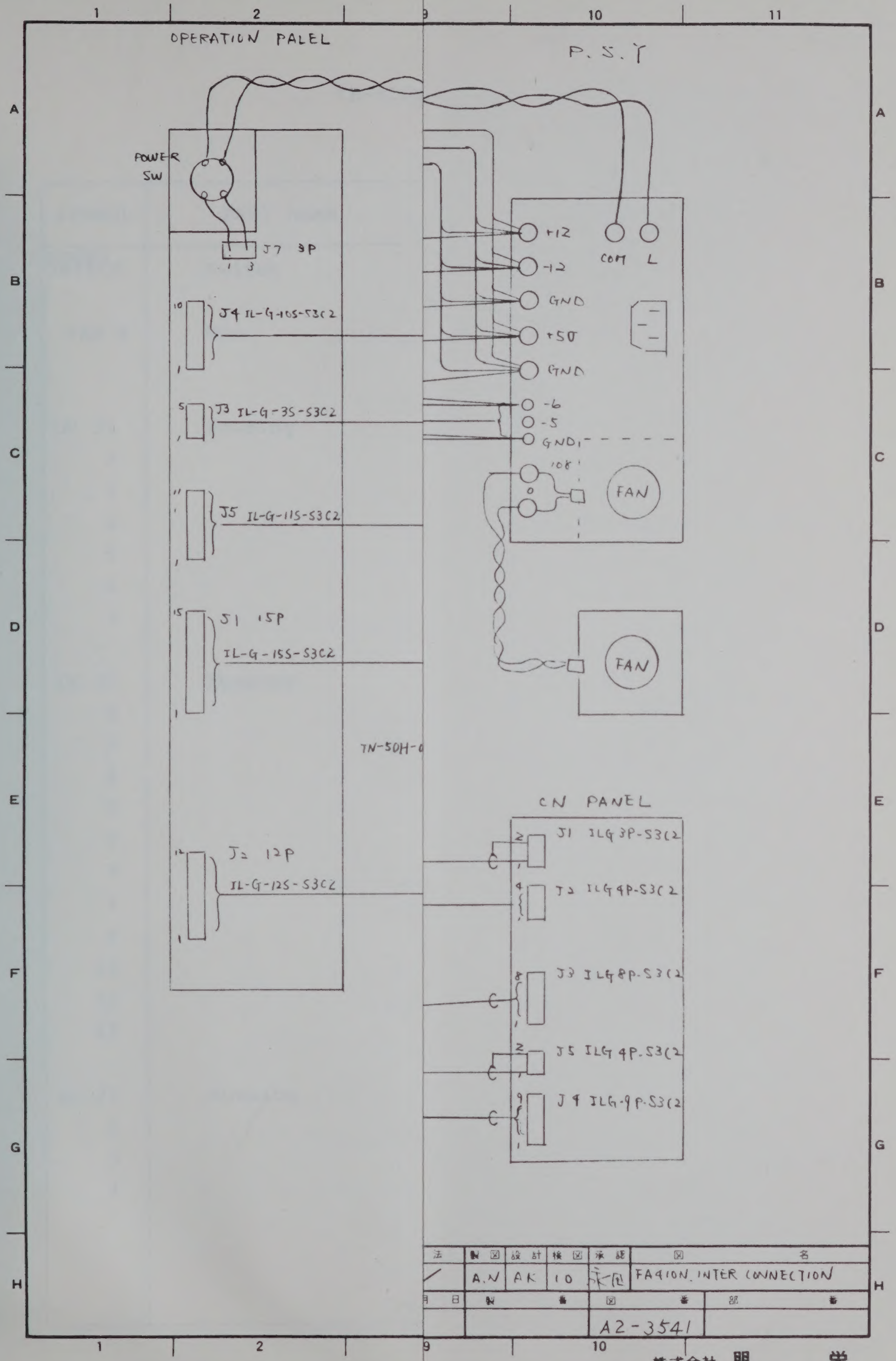
OPERATION PALEL
P.S.Y
POWER SW
J7 3P
1 3
J4 IL-G-10S-S3C2
J3 IL-G-3S-S3C2
J5 IL-G-11S-S3C2
J1 15P
IL-G-15S-S3C2
J2 12P
IL-G-12S-S3C2
7N-50H-0
+12
-12
GND
+5V
GND
-6
-5
GND1
108
0
COM
L
FAN
FAN
CN PANEL
J1 ILG 3P-S3C2
J2 ILG 4P-S3C2
J3 ILG 8P-S3C2
J5 ILG 4P-S3C2
J4 ILG-9P-S3C2
1
2
9
10
11
A
B
C
D
E
F
G
H

法	製図	設計	検図	承認	図名
/	A.N	AK	10	永田	FA410N INTER CONNECTION
日	製番		図番	部番	
			A2-3541		

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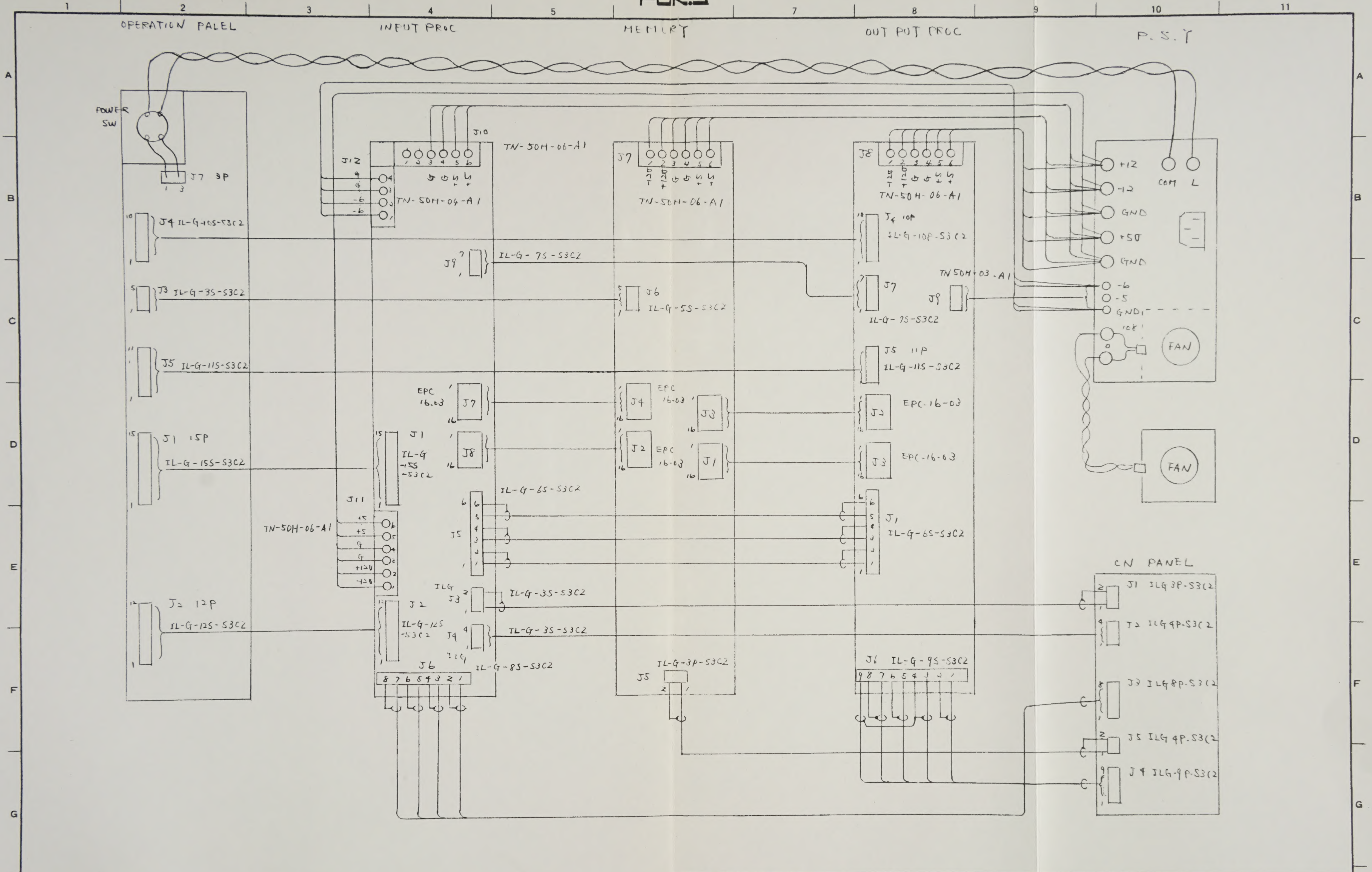
FOR.A


OPERATION PALEL
INPUT PROC
MEMORY
OUT PUT PROC
P. S. Y
POWER SW
J7 3P
J4 IL-G-10S-S3C2
J3 IL-G-3S-S3C2
J5 IL-G-11S-S3C2
J1 15P
IL-G-15S-S3C2
J2 12P
IL-G-12S-S3C2
J10
TN-50H-06-A1
J12
TN-50H-04-A1
J9 IL-G-7S-S3C2
EPC 16-03
J7
J8
J1 IL-G-15S-S3C2
J11
TN-50H-06-A1
+5
G
+12U
-12U
J5 IL-G-6S-S3C2
ILG J3 IL-G-3S-S3C2
J2 IL-G-12S-S3C2
ILG J4 IL-G-3S-S3C2
J6 IL-G-8S-S3C2
J7 TN-50H-06-A1
J6 IL-G-5S-S3C2
J4 EPC 16-03
J3
J2 EPC 16-03
J1
J5 IL-G-3P-S3C2
J8 TN-50H-06-A1
J4 10P IL-G-10P-S3C2
J7 IL-G-7S-S3C2
TN 50H-03-A1
J9
J5 11P IL-G-11S-S3C2
J2 EPC-16-03
J3 EPC-16-03
J1 IL-G-6S-S3C2
J6 IL-G-9S-S3C2
+12
-12
GND
+5U
GND
COM
L
-6
-5
GND
10K
FAN
FAN
CN PANEL
J1 ILG 3P-S3C2
J2 ILG 4P-S3C2
J3 ILG 8P-S3C2
J5 ILG 4P-S3C2
J4 ILG 9P-S3C2

改訂	A	第三角図法	製図	設計	検図	承認	図名
		尺度 /	A.N	AK	10	永田	FA410N. INTER CONNECTION
		作成 年 月 日	製番			図番	部番
		個数				A2-3541	

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FA-410N HARNESS

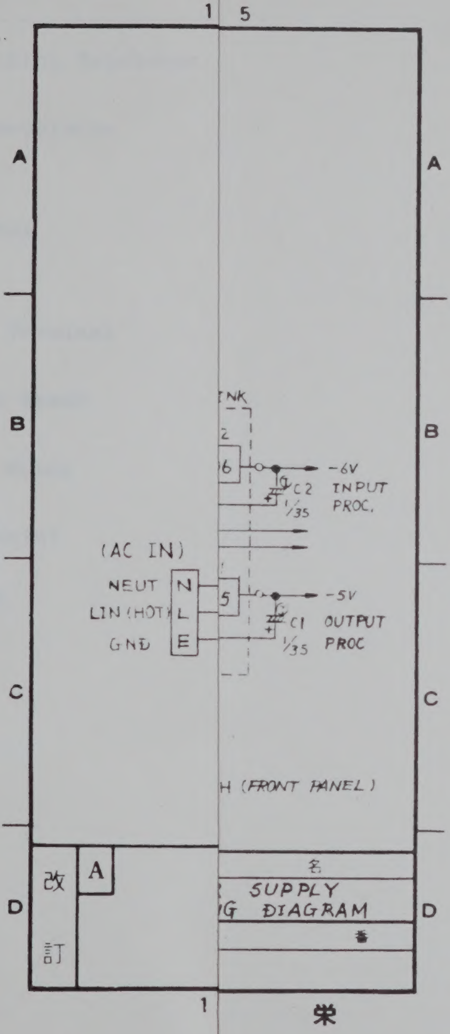
1/2

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
POWER SWITCH	Switch	DHA-1S8GB	
FAN 2	Fun	109-043 UL	
OP J1	Housing	IL-G-15S-S3C2	
2		-12S-	
3		- 5S-	
4		-10S-	
5		-11S-	
6		Deleted	
7		IL-G-3S-S3C2	
IN J1	Housing	IL-G-15S-S3C2	
2		-12S-	
3		- 3S-	
4		- 4S-	
5		- 6S-	
6		- 8S-	
7		FCP-16-03	
8		"	
9		IL-G-7S-S3C2	
10		TN-50H-06-A1	
11		"	
12		-04-	
ME J1	Housing	FCP-16-03	
2		"	
3		"	
4		"	

FA-410N HARNESS

2/2

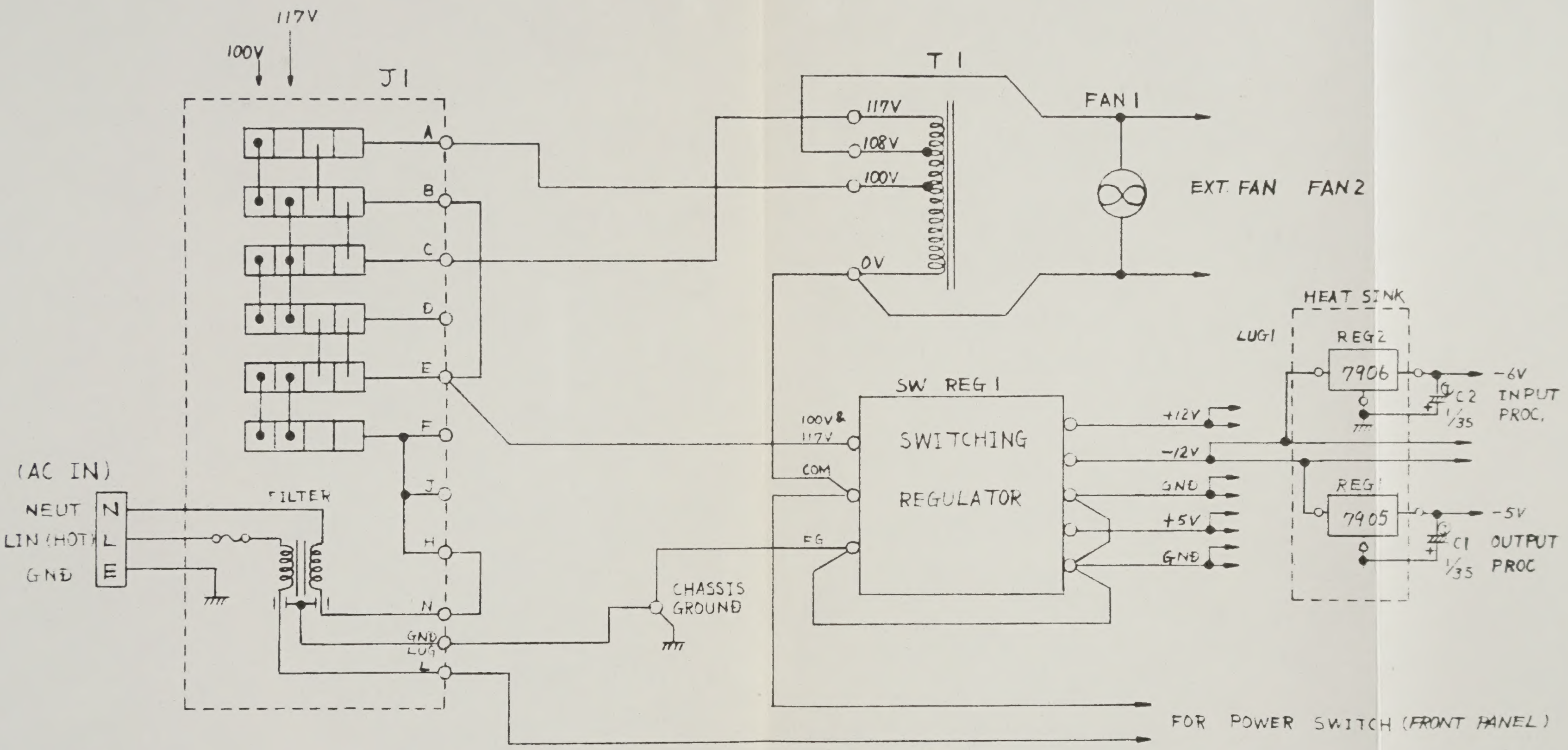
SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
ME J5	Housing	IL-G-3S-S3C2	
6		-6S-	
7		TN-50H-06-A1	
OUT J1	Housing	IL-G-6S-S3C2	
2		ECP-16-03	
3		"	
4		IL-G-10S-S3C2	
5		-11S-	
6		- 9S-	
7		- 7S-	
8		TN-50H-06-A1	
9		-03-	
CN J1	Housing	IL-G-3S-S3C2	
2		-4S-	
3		-8S-	
4		-9S-	
5		-4S-	
Contact	for IL-G	IL-G-C2-5000	
Power Supply	Power	A4-2361-1	
	Connector	1625-02R1 1625-02P1	
Switch Card	Substrate	A4 2359	
Input Processor		A2-3488~3492	
OUTPUT Processor		A2-3443~3446	
Memoty DOC		A2-3407~3410	
Connector Board		A2-3438	
		A2-3439	
Operation Panel		A3-2811	


1
5
A
B
C
D
INK
2
6
-6V
C2
INPUT
PROC.
1/35
(AC IN)
NEUT
LIN (HOT)
GND
N
L
E
5
-5V
C1
OUTPUT
PROC
1/35
H (FRONT PANEL)
改
訂
A
名
SUPPLY
IG DIAGRAM
番
1
栄

FA-410N HARNESS

2/2

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
ME J5	Housing	IL-G-3S-S3C2	
6		-6S-	
7		TN-50H-06-A1	
OUT J1	Housing	IL-G-6S-S3C2	
2		ECP-16-03	
3		"	
4		IL-G-10S-S3C2	
5		-11S-	
6		- 9S-	
7		- 7S-	
8		TN-50H-06-A1	
9		-03-	
CN J1	Housing	IL-G-3S-S3C2	
2		-4S-	
3		-8S-	
4		-9S-	
5		-4S-	
Contact	for IL-G	IL-G-C2-5000	
Power Supply	Power	A4-2361-1	
	Connector	1625-02R1 1625-02P1	
Switch Card	Substrate	A4 2359	
Input Processor		A2-3488~3492	
OUTPUT Processor		A2-3443~3446	
Memoty DOC		A2-3407~3410	
Connector Board		A2-3438	
Operation Panel		A2-3439 A3-2811	


117V
100V
J1
A
B
C
D
E
F
J
H
N
GND LUG
L
(AC IN)
NEUT
LIN (HOT)
GND
N
L
E
FILTER
CHASSIS GROUND
T1
117V
108V
100V
0V
FAN1
EXT. FAN
FAN2
SW REG1
SWITCHING REGULATOR
100V & 117V
COM
FG
+12V
-12V
GND
+5V
GND
HEAT SINK
LUG1
REG2
7906
C2
1/35
-6V
INPUT PROC.
REG1
7905
C1
1/35
-5V
OUTPUT PROC
FOR POWER SWITCH (FRONT PANEL)

改訂 A

第三角図法	製図	設計	検図	承認	図名
尺度 /	T.Y	I. SATTO			FA410(N POWER SUPPLY WIRING DIAGRAM
作成57年6月18日	製番		図番		部番
個数			A4 - 2361 - 1		

株式会社 朋栄

FA-410N POWER SUPPLY

1/1

SYMBOL	PART NAME	DESCRIPTIONS	REMARKS
SW.REG1	Swithing Regulator	FP-1	
REG 1	IC Regulator	7905	
REG 2	"	7906	
C 1	Tantal	1μF 35V	
C 2	"	"	
LUG 1	Lag Terminal	L3552 1L6P	
T 1	Auto Trans	PT-1145	
FAN 1	Fun MOter	109-043UL	
J 1	AC Inlet	6J4	
	FUSE	UL. CSA 6.3×32 SLO-BLO 3A	